CSC258H5S Winter 2015 Midterm
Duration — 50 minutes

Student Number: _____

Last Name: KEY **First Name:** _____

*Do **not** turn this page until you have received the signal to start.*
(Please fill out the identification section above and read the instructions below.)
Good Luck!

This midterm consists of 3 questions on 8 pages (including this one and two blank pages at the back). *When you receive the signal to start, please make sure that your copy is complete.*

Please write legibly and provide succinct, well-structured answers.

If you use any space for rough work, indicate clearly what you want marked. It is beneficial to show your work, so that we can interpret your answers and award partial credit.

If you are uncertain about how to answer a question, write down your assumptions and then solve the problem based on those assumptions.

If you wish to detach the final page of the test (the blank pages), you may. Be very sure to indicate if you want any part of the blank pages marked; otherwise, we will treat them as scrap paper.

1: _____/ 9

2: _____/ 6

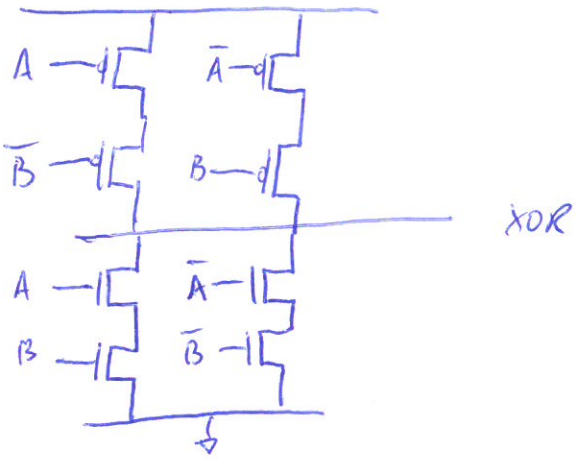
3: _____/ 5

TOTAL: _____/20

Question 1. Short Answer [9 MARKS]

Part (a) Transistors [2 MARKS]

Sketch a transistor-level circuit for a 2-input CMOS XOR gate. You may use A, $\overline{A}$, B, and $\overline{B}$ as inputs to the transistors. (i.e., You don't need to implement a CMOS NOT gate.)



+1 correct CMOS structure

+1 correct XOR

Part (b) Two's Complement Arithmetic [1 MARK]

Showing your work, add 10110001 and 11010110. Indicate whether or not the sum overflows.

```
 1 1 1 1
  10110001
+ 11010110
-----------
1 10000111
```

No overflow

+1, correct answer, no overflow.

Part (c) Two's Complement Arithmetic [1 MARK]

(0.5 for correct answer but "overflow")

Showing your work, subtract 00110001 from 10010110. Indicate whether or not the computation overflows.

```
00110001 => 11001111
 (negate)

  1 1 1
  10010110
+ 11001111
-----------
1 01100101
```

Overflow

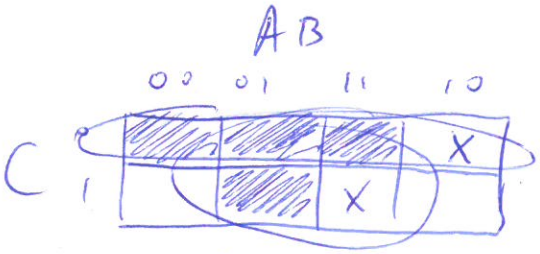
+0.5 negation

+0.5 overflow detected

Part (d) K-Maps [2 MARKS]

Use a Karnaugh map to simplify the function described in the truth table below. Provide the k-map and the optimized formula you derive from it.

A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	X
1	0	1	0
1	1	0	1
1	1	1	X



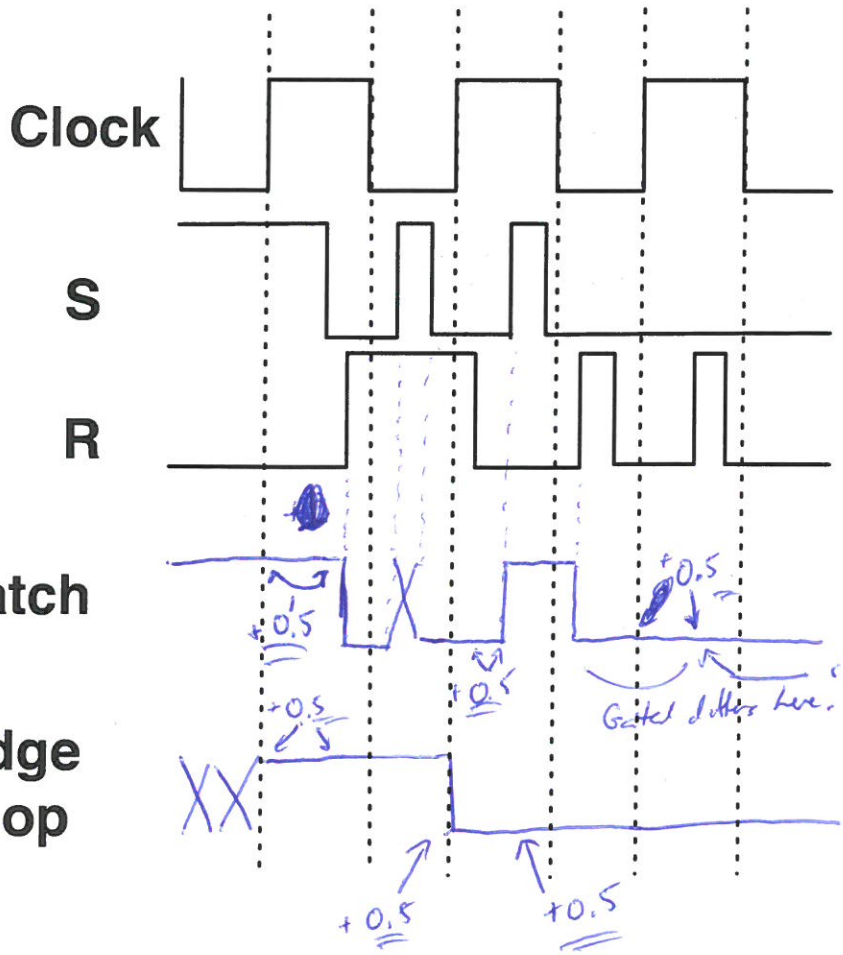
$\bar{C} + B$

+1 correctly setup k-map

+1 correctly extracted formula

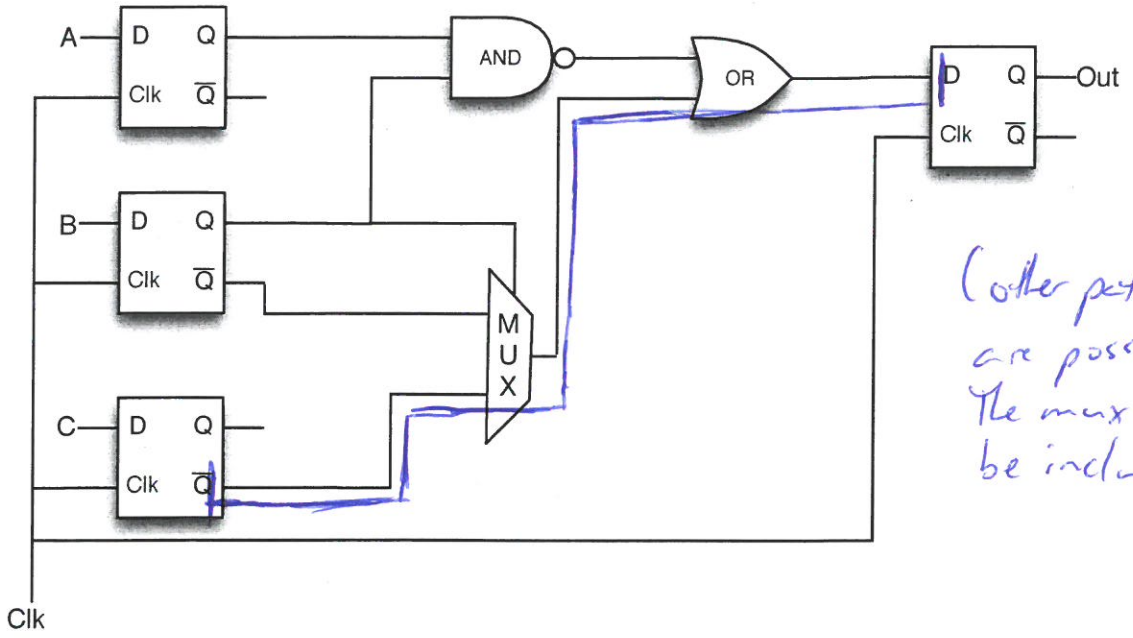
Part (e) Timing [3 MARKS]

Given the input waveform below, sketch the output, Q, of an SR latch and an SR flip-flop.



Non-gated is drawn. gated is fine, too

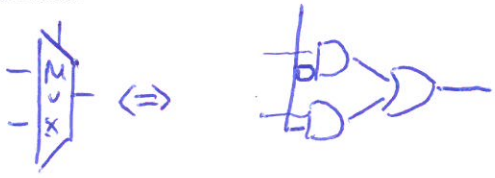
Question 2. Circuit Analysis [6 MARKS]



(other paths are possible. The mux must be included)

For the following subquestions, use the circuit above and assume that each 2-input boolean gate has a propagation delay of 30 ns and contamination delay of 15 ns. (NOT gates are free.) Assume that a D flip-flop has a clock-to-q propagation delay of 80 ns, setup time of 120 ns, hold time of 70 ns, and clock-to-q contamination delay of 40 ns.

Part (a) [2 MARKS] What are the propagation and contamination delays of the 2-1 multiplexer used in the circuit?



Prop: 2 gates

$30 \times 2 = \boxed{60\text{ ns}}$ +1

Cont: 2 gates

$15 \times 2 = \boxed{30\text{ ns}}$ +1

(wrong design, right computation: +1 only)

Part (b) [2 MARKS] What is the propagation delay of the full sequential circuit on the previous page? Please identify the longest path (by highlighting it on the circuit schematic) and show your work.

path : +1

prop delay : +1

prop : $T_{pcq} + T_{PD} + T_{setup}$

$80 + 3 \times 30 + 120$

$80 + 90 + 120$

$\boxed{290}$

Part (c) [1 MARK] Does the circuit above contain a hold time violation? Explain why or why not.

justification : +1

hold time $\leq T_{ccq} + T_{CD}$

$70 \leq 40 + 2 \times 15$

$70 \leq 70$ ✓ No violation.

'Short-path Delay is equal to hold time.

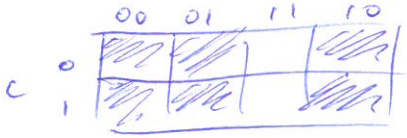
Part (d) [1 MARK] This circuit has a simpler representation. Provide a simpler boolean formula for the combinational portion of the circuit. Show the work you performed to arrive at the simpler circuit.

The mux can be read in two ways. Assuming the top input is selected on a 0:

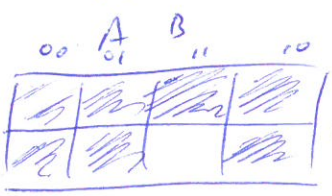
$\overline{A}B + (\overline{B}\,\overline{B} + B\overline{C}) \Rightarrow \overline{A} + \overline{B} + \overline{B} + B\overline{C}$

If the top input is selected on a 1:

$\overline{A}B + (B\overline{B} + \overline{B}\,\overline{C}) \Rightarrow \overline{A} + \overline{B} + \overline{B}\,\overline{C}$



$\Rightarrow \overline{A} + \overline{B} = \overline{AB}$



$\Rightarrow \overline{A} + \overline{B} + \overline{C} = \overline{ABC}$

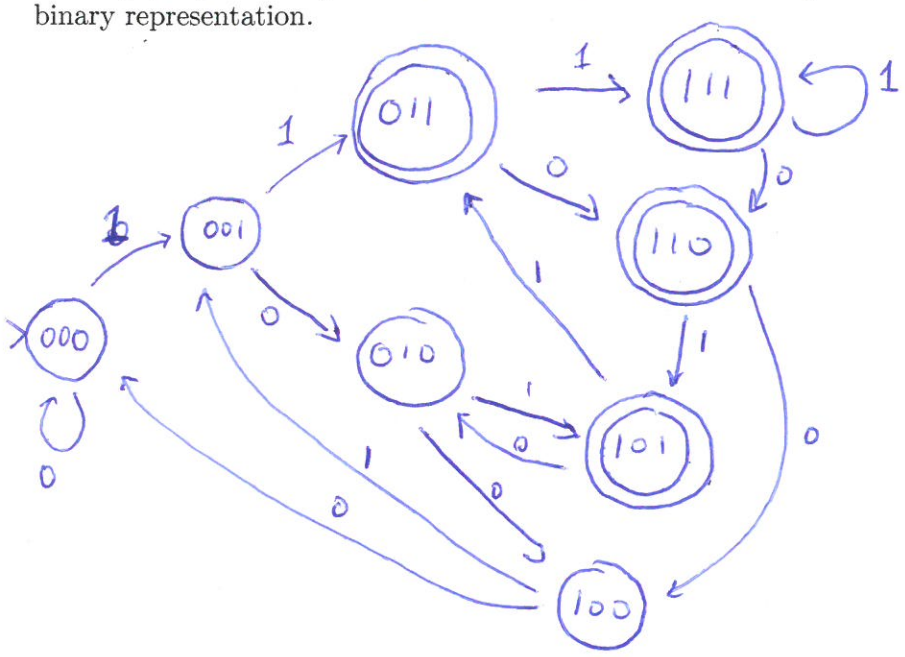
+1 justified process

CONT'D...

Question 3. Finite State Machines [5 MARKS]

In this problem, you will be exploring the design of a FSM with two inputs – A and a *clock* – and one output – *alert*. *alert* should be 1 if A has been 1 in at least two of the previous three cycles.

Part (a) [3 MARKS] Draw the Moore state transition diagram for this FSM. Label each state with its binary representation.



Clock is implied. Each transition occurs on the clock edge.

Alert is 1 in accepting (double circle) states.

+1 tree-based structure
+1 "alert" correctly set
+1 transitions on "A"

Part (b) [2 MARKS] Provide the state transition table and output table for this FSM.

state	A	state'
000	0	000
000	1	001
001	0	010
001	1	011
010	0	100
010	1	101
011	0	110
011	1	111
100	0	000
100	1	001
101	0	010
101	1	011
110	0	100
110	1	101
111	0	110
111	1	111

state	alert
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1

+1 transition table matches (a)
+1 output table matches (a), is moore

CONT'D...