CSC258H5S Winter 2014 Midterm
Duration — 50 minutes

Student Number: |_|_|_|_|_|_|_|_|_|_|

Last Name: _____ **First Name:** _____

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*Do **not** turn this page until you have received the signal to start.*
(Please fill out the identification section above and read the instructions below.)
Good Luck!

This midterm consists of 3 questions on 8 pages (including this one). *When you receive the signal to start, please make sure that your copy is complete.*

Please write legibly and provide succinct, well-structured answers.

If you use any space for rough work, indicate clearly what you want marked. It is beneficial to show your work, so that we can interpret your answers and award partial credit.

If you are uncertain about how to answer a question, write down your assumptions and then solve the problem based on those assumptions.

Marks

1: _____/ 8
2: _____/ 5
3: _____/ 7
TOTAL: _____/20

Question 1. Short Answer [8 MARKS]

Part (a) Two's Complement [1 MARK]

Convert the decimal number -19 to 6-bit 2's complement form or indicate that the decimal number would overflow the range.

Part (b) Arithmetic [1 MARK]

Add the two's complement numbers 10101110 and 11100100. Indicate whether or not the sum overflows.

Part (c) Transistors [1 MARK]

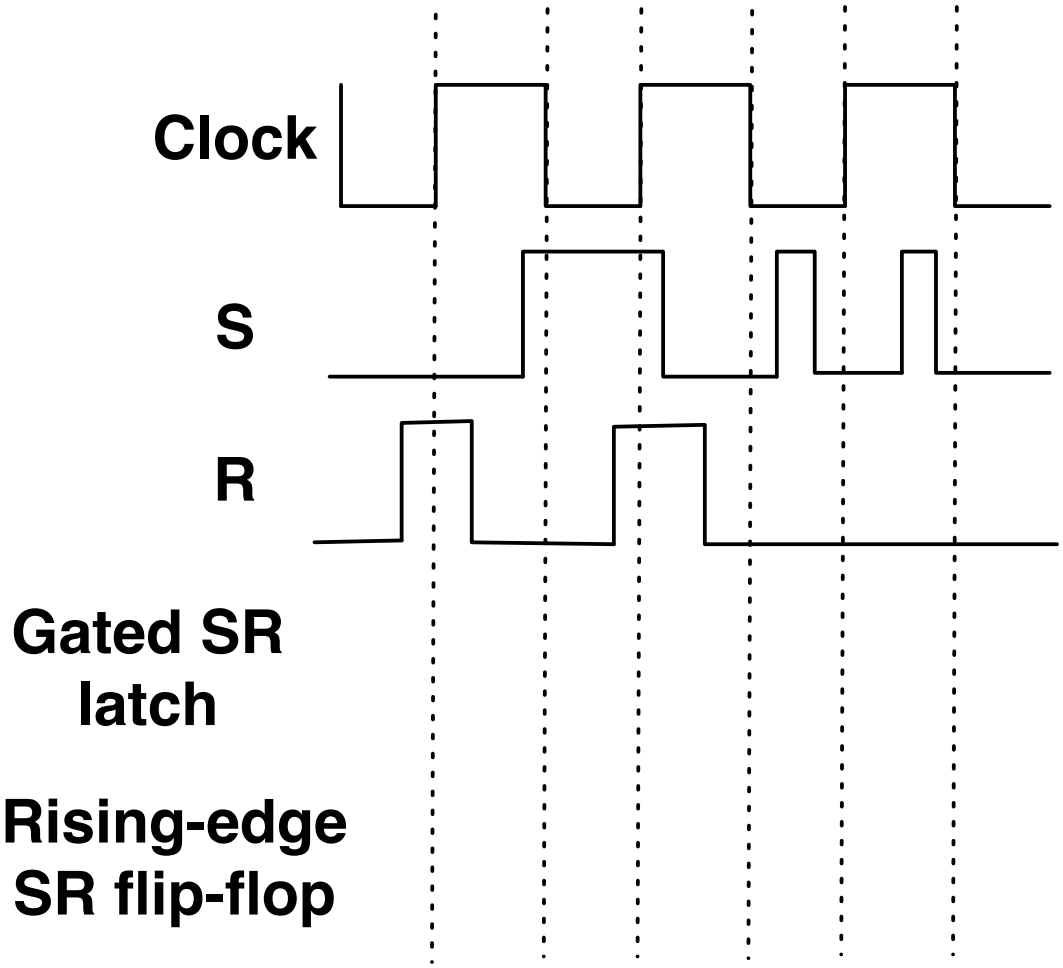
Sketch a transistor-level circuit for a CMOS NOR gate.

Part (d) Processors [3 MARKS]

Succinctly explain how the MIPS processor from the text selects and obtains instructions to execute.

Part (e) Timing [2 MARKS]

Given the input waveform below, sketch the output, Q, of an SR latch and SR flip-flop.



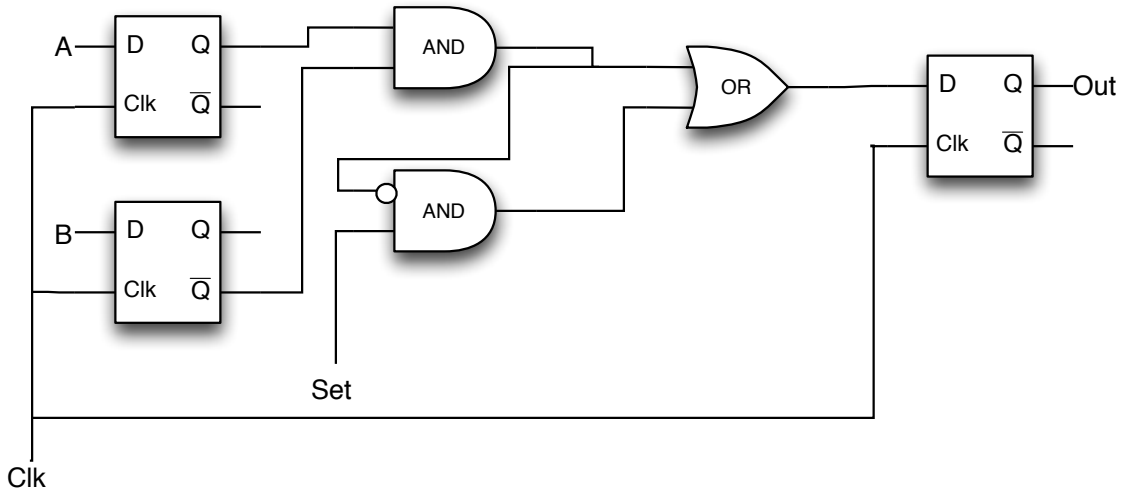
Question 2. Logic Design and Latency [5 MARKS]

Part (a) [2 MARKS] Provide the truth table for the formula $\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BD + AB\bar{C}D$.

Part (b) [3 MARKS] Use a Karnaugh map to optimize the formula from part (a). Provide the Karnaugh map and the optimized formula.

Question 3. Sequential Circuits [7 MARKS]

Part (a) [4 MARKS] A JK flip-flop functions like an SR flip-flop except in the case where S and R are both 1. In that situation, an SR flip-flop's behaviour is undefined, but a JK flip-flop toggles its state (like a T flip-flop). Sketch the schematic for a positive-edge JK flip-flop. Use only SR *latches* and basic boolean logic gates. (*Hint:* You may wish to use a master-slave configuration to build your flip-flop.)



For the following subquestions, use the circuit above and assume that each 2-input boolean gate has a propagation delay of 30 ns and contamination delay of 20 ns. (NOT gates are free.) Assume that a D flip-flop has a clock-to-q propagation delay of 80 ns, setup time of 120 ns, hold time of 75 ns, and clock-to-q contamination delay of 40 ns.

Part (b) [2 MARKS] What is the propagation delay of the circuit above? Please identify the longest path (by highlighting it on the circuit schematic) and show your work.

Part (c) [1 MARK] The timing analysis we have done in class has not considered *wire delay*: the time required for signals to traverse wires between gates or devices. Wire delay is difficult to predict, so designers are often given a *maximum wire delay* parameter that is the largest amount of wire-related delay that could be added to any path in the circuit.

a. Does wire delay factor into the calculation of propagation delay? If so, how?

b. Does wire delay factor into the calculation of contamination delay? If so, how?