Last Name: _____ **First Name:** _____

Student #: |_|_|_|_|_|_|_|_|_|_| **Signature:** _____

UNIVERSITY OF TORONTO MISSISSAUGA
APRIL 2014 FINAL EXAMINATION
CSC258H5S
Computer Organization
Andrew Petersen
Duration - 3 hours
Aids: None

The University of Toronto Mississauga and you, as a student, share a commitment to academic integrity. You are reminded that you may be charged with an academic offence for possessing any unauthorized aids during the writing of an exam. Clear, sealable, plastic bags have been provided for all electronic devices with storage, including but not limited to: cell phones, tablets, laptops, calculators, and MP3 players. Please turn off all devices, seal them in the bag provided, and place the bag under your desk for the duration of the examination. You will not be able to touch the bag or its contents until the exam is over.

If, during an exam, any of these items are found on your person or in the area of your desk other than in the clear, sealable, plastic bag; you may be charged with an academic offence. A typical penalty for an academic offence may cause you to fail the course.

*Please note, you **CANNOT** petition to **re-write** an examination once the exam has begun.*

This final examination consists of 6 questions on 18 pages (including this one). When you receive the signal to start, please make sure that your copy of the examination is complete.

If you need more space for one of your solutions, use the last pages of the exam and indicate clearly the part of your work that should be marked.

Marking Guide

1: _____/16

2: _____/ 5

3: _____/ 9

4: _____/ 9

5: _____/12

6: _____/ 9

TOTAL: _____/60

CONTINUED ON PAGE 2

16 marks **Question 1.** Short Answer

1 mark **Part (a)** Binary Numbers

Provide the 6-bit two's complement representation for the decimal number -11.

2 marks **Part (b)** Binary Arithmetic

Define *overflow* in the context of binary arithmetic and explain how a hardware adder detects it.

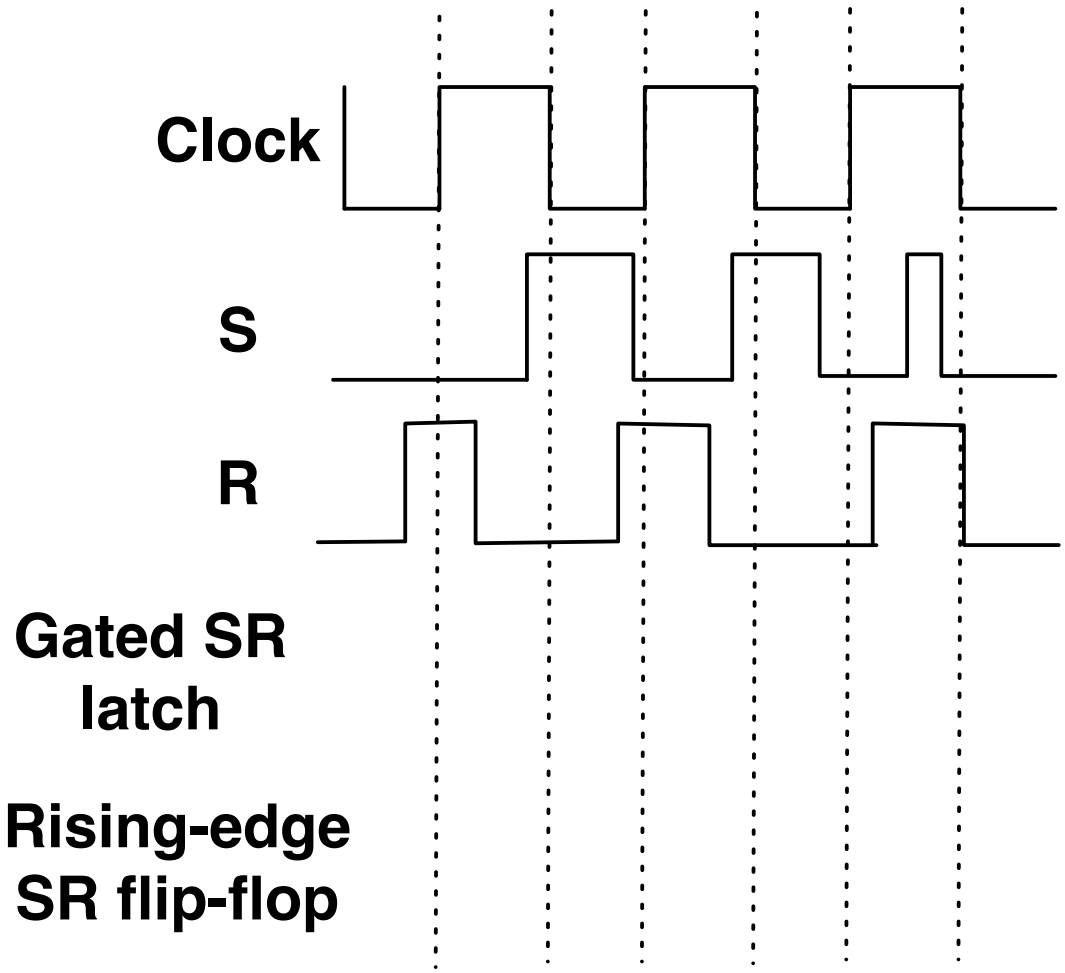
1 mark **Part (c)** Arithmetic Circuits

Explain how a prefix adder computes the sum of two numbers more quickly than a ripple-carry adder.

CONTINUED ON PAGE 3

2 marks **Part (d)** Timing

Given the input waveform below, sketch the output, Q, of an SR latch and SR flip-flop.



2 marks **Part (e)** FSMs and Processors

Explain how the MIPS processor in the textbook is a finite state machine.

CONTINUED ON PAGE 4

3 marks **Part (f)** Processors

Succinctly explain how the MIPS processor from the text uses the program counter (PC) to select instructions. Also explain how the PC is updated.

1 mark **Part (g)** Processors and Machine Code

The MIPS I-type encoding includes space for a 16-bit immediate. That value is often zero-extended or sign-extended. Why?

CONTINUED ON PAGE 5

2 marks **Part (h)** Exceptions

Describe what occurs on a MIPS machine when the user invokes a *system call*.

2 marks **Part (i)** Memory Model

Explain what kind of values are stored in each of the following sections of memory.

a. Stack

b. Heap

c. Global Data Segment

d. Text Segment

CONTINUED ON PAGE 6

5 marks **Question 2.** Logic Design

1 mark **Part (a)** Truth Tables

Produce the truth table for a 1-bit 2-1 multiplexer. *Recall:* A multiplexer takes a control input *select* as well as data inputs. It has a single output that carries the value of the selected data input.

2 marks **Part (b)** K-Maps

Use a Karnaugh map to simplify the function described in your multiplexer truth table. Provide the k-map and the optimized formula you derive from it.

CONTINUED ON PAGE 7

A	B	C	D	Out
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	1
1	0	0	0	X
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

2 marks

Part (c) K-Maps

Use a Karnaugh map to simplify the function described in the truth table above. Provide the k-map and the optimized formula you derive from it.

CONTINUED ON PAGE 8

9 marks **Question 3.** Register Design

2 marks **Part (a)** Latches and Flip-flops

Succinctly describe the key difference between a latch and a flip-flop. Then, explain why flip-flops are preferred for most circuit implementations.

1 mark **Part (b)** SR Latch

Provide the truth table and characteristic equation for an (ungated) SR latch.

2 marks **Part (c)** D Flip-flop

Using a master-slave configuration, draw the circuit diagram for a positive-edge D flip-flop. You may only use ungated SR latches and basic logic gates.

CONTINUED ON PAGE 9

4 marks

Part (d) Register

Draw the circuit diagram for a 4-bit register that takes a 4-bit *data* input, *clock*, *enable* command, *shift* command, and *reset* command. The device only operates on the positive edge of the clock:

- If the *enable* signal is high and *shift* is low, the register stores the value on the *data* input.
- When *shift* and *enable* are both high, the register performs a left circular shift on the currently stored data, rather than accepting a new value from the *data* input.
- When *enable* is low, the register does not accept a new state (except as below).
- If *reset* is high, the state of the register is set to 0000, regardless of the values of *data* and *enable*.

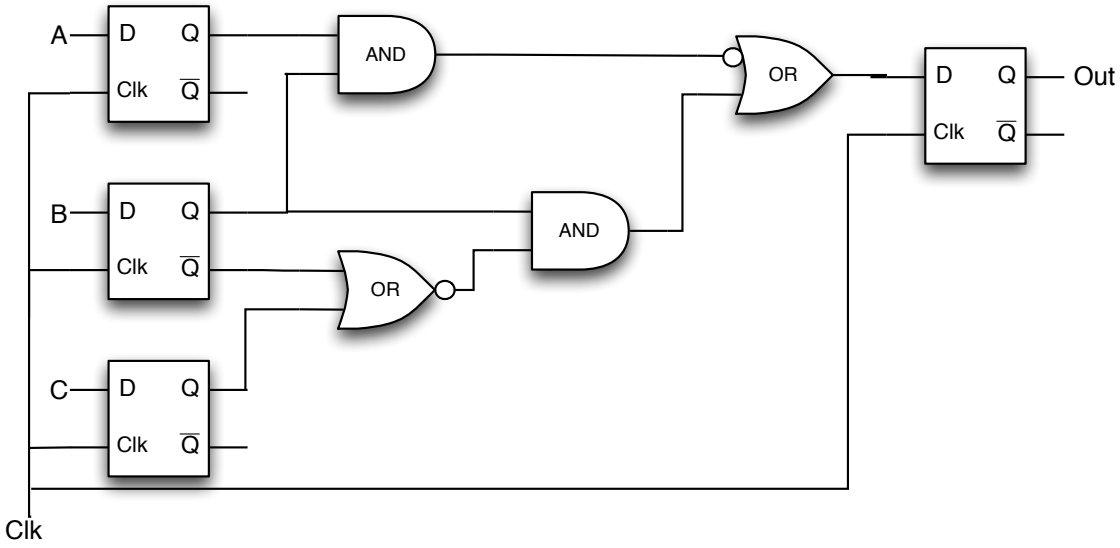
You may only use 1-bit D flip-flops (without reset and enable), multiplexers or demultiplexers of any size, and basic logic gates to build your register.

CONTINUED ON PAGE 10

9 marks

Question 4. Latency

For the following questions, assume that each 2-input boolean gate has a propagation delay of 30 ns and contamination delay of 10 ns. (NOT gates are free.) Assume that a D flip-flop has a clock-to-q propagation delay of 80 ns, setup time of 120 ns, hold time of 75 ns, and clock-to-q contamination delay of 30 ns.



2 marks

Part (a) Sequential Logic Propagation Delay

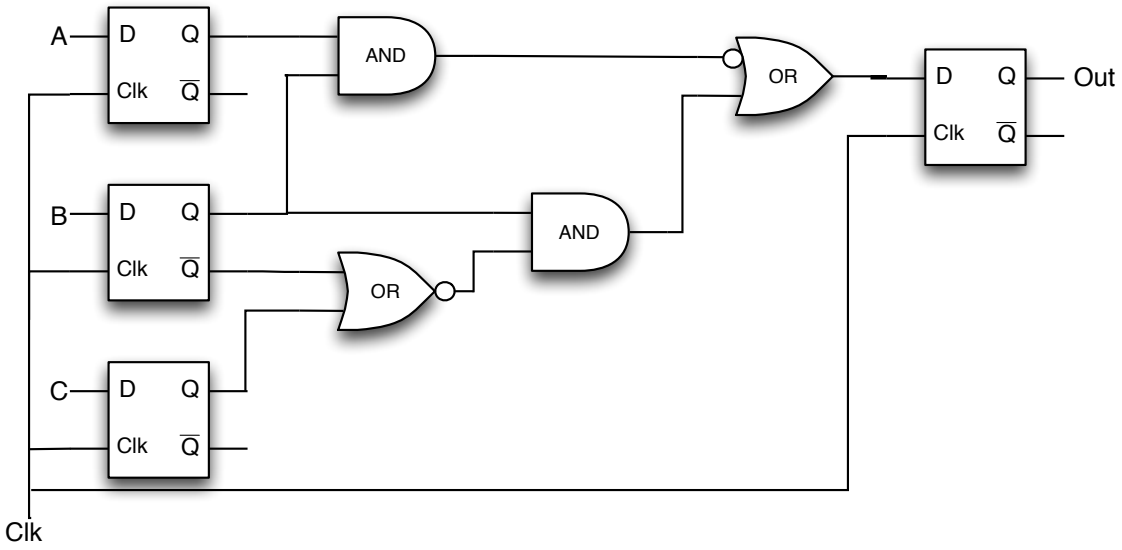
What is the clock-to-q propagation delay of the circuit above? Please identify the longest path (by highlighting it on the circuit schematic) and show your work.

1 mark

Part (b) Clock Skew

What is the propagation delay of the circuit if the circuit can experience up to 20 ns of skew?

CONTINUED ON PAGE 11



2 marks **Part (c)** Contamination Delay

What is the contamination delay of the circuit above? Please identify the shortest path (by highlighting it on the circuit schematic) and show your work.

2 marks **Part (d)** Hold Time

Is there the possibility of a hold time violation in this circuit? Explain why or why not.

2 marks **Part (e)** Clock Skew

First, what is the contamination delay of the circuit if the circuit can experience up to 20 ns of skew? Second, does that change your answer to the previous question about hold time violations? Explain why or why not.

CONTINUED ON PAGE 12

12 marks **Question 5.** Machine and Assembly Code

2 marks **Part (a)** Instruction Set Architectures

The MIPS instruction set only operates on values in registers and in immediate fields – not (directly) on values in memory. Recalling what you know about the impact of memory on performance *and* the factors that influence good ISA design, explain why.

2 marks **Part (b)** Compiler Tool Chain

What is the purpose of the *linker*?

CONTINUED ON PAGE 13

4 marks **Part (c)** Function Calls

List the steps required in the function call convention that you learned about in lab (from Larus's text).

CONTINUED ON PAGE 14

2 marks **Part (d)** Assembly Programming

Provide the MIPS assembly code that assigns 2 to register $t2 if the value in register $t0 is 0 and that assigns $t1 + 2 to $t2 otherwise. If you do not remember the opcode for an instruction that you want to use, write a comment that explains what the assembly operation should do.

2 marks **Part (e)** Assembly Programming

Provide the MIPS assembly code that allocates an integer array of length 6 on the stack and then assigns the value 42 to each element in the array. If you do not remember the opcode for an instruction that you want to use, write a comment that explains what the assembly operation should do.

CONTINUED ON PAGE 15

9 marks **Question 6.** Caches

2 marks **Part (a)** Caches

Briefly explain why a cache system is an key piece of a modern processor.

2 marks **Part (b)** Locality

Define the term *locality* and explain how it is related to caching.

CONTINUED ON PAGE 16

2 marks **Part (c)** Associativity

List the advantages and disadvantages of a fully-associative cache, as compared to a direct-mapped cache.

3 marks **Part (d)** Cache Impact

You are part of a team that is building a vector processor for a specific, well-understood application workload. For the expected workload, 20% of the instructions in the workload are `load` operations, and another 15% are `store` operations. The cache your team has designed would have an 90% hit rate and a latency of 3 processor cycles. In contrast, a memory access would take 150 processor cycles. Unfortunately, your team's manager is concerned about the cost of the cache. Write a single paragraph that presents a succinct, well-organized argument for including the cache in the final processor design. Your argument should use the calculation of average memory access time (AMAT) and cycles per instruction (CPI) as evidence.

Total Marks = 60

CONTINUED ON PAGE 17

*[Use the space below for rough work. This page will **not** be marked, unless you clearly indicate the part of your work that you want us to mark.]*

CONTINUED ON PAGE 18

*[Use the space below for rough work. This page will **not** be marked, unless you clearly indicate the part of your work that you want us to mark.]*