CSC258H5S Winter 2013 Midterm
Duration — 50 minutes

**Student Number:** |_|_|_|_|_|_|_|_|_|_|

**Last Name:** _____ **First Name:** _____

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*Do **not** turn this page until you have received the signal to start.*
(Please fill out the identification section above and read the instructions below.)
*Good Luck!*

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This midterm consists of 3 questions on 10 pages (including this one). *When you receive the signal to start, please make sure that your copy is complete.*

You are allowed one 8.5x11 sheet of paper filled with *your* notes.

If you use any space for rough work, indicate clearly what you want marked.

If you are uncertain about how to answer a question, write down your assumptions and then solve the problem based on those assumptions.

# 1: _____/ 6

# 2: _____/ 8

# 3: _____/ 6

TOTAL: _____/20

## Question 1. Short Answer [6 MARKS]

### Part (a) Transistors [1 MARK]

Sketch the CMOS implementation of a three-input NOR gate.

### Part (b) 2's Complement [1 MARK]

What is the result of adding the 2's complement numbers 0001 and 1111?

**Part (c)** Latches and Flip-Flops [2 MARKS]

What is the difference between a latch and a flip-flop? Why are flip-flops preferred over latches in almost all applications?

**Part (d)** Parallelism [2 MARKS]

In the context of this course, what is "parallelism"? How do "spatial" and "temporal" (pipelining) parallelism differ?

## Question 2. Logic Design and Latency [8 MARKS]

**Part (a)** [2 MARKS] Provide the truth table and schematic for the formula $(A + B + C)(\bar{A} + B + \bar{C})$.

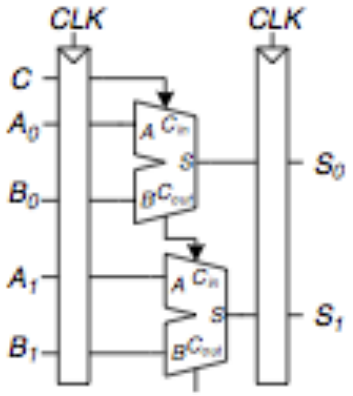
| $A$ | $B$ | $C$ | $D$ | $Out$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | X |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | X |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | X |

**Part (b)** [2 MARKS] Use a Karnaugh map to simplify the function described in the truth table above. Provide the k-map and the optimized formula you derive from it.

**Part (c)** [2 MARKS] If any gate (XOR or not!) has a propagation delay of 15 ns and a contamination delay of 5 ns, then:

(a) What is the propagation delay of a full adder?

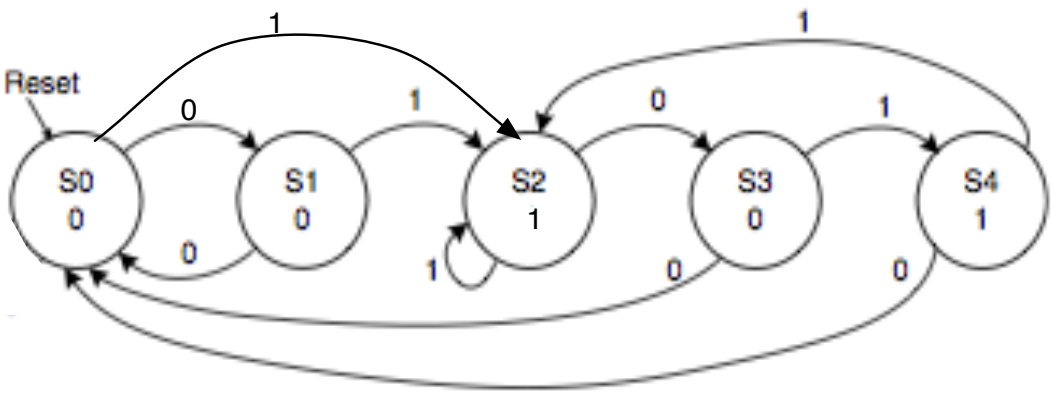
(b) What is the contamination delay of a full adder?




**Part (d)** [1 MARK] Using the full adder latency and contamination delay you calculated and assuming that D flip-flops have a propagation delay of 30 ns and a setup time of 10 ns, what is the minimum clock period of the circuit above?

**Part (e)** [1 MARK] Using the full adder latency and contamination delay you calculated and assuming that D flip-flops have a propagation delay of 30 ns and a hold time of 20 ns, what is the maximum clock skew that the circuit above can tolerate?

**Question 3.** Finite State Machines [6 MARKS]




**Part (a)** [3 MARKS] Using a one-hot state encoding, complete the state transition table and output table for the FSM above.

**Part (b)** [1 MARK] Sketch the schematic for the FSM at the beginning of this problem. You may use any gates that you need as well as D flip-flops.

**Part (c)** [2 MARKS] Sketch the state diagram for a Mealy state machine that computes the *parity* of the sequence of values observed on an input *A* since the last *reset* signal was received. If the parity of the sequence is even, then the FSM outputs True (1). Otherwise, it outputs False (0). When a *reset* signal is received, the machine re-initializes.

Note: The parity of a sequence of binary digits is even if the number of 1's observed is even, and the parity is odd if the number of observed 1's is odd. For example, if the input A takes the values 1, 0, 1, 0, 0, 1 over six cycles, then the parity is odd on the first, second, and sixth cycles and even on the third, fourth, and fifth cycles.

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