Last Name: _____ **First Name:** _____

Student #: |_|_|_|_|_|_|_|_|_|_| **Signature:** _____

UNIVERSITY OF TORONTO MISSISSAUGA
APRIL 2013 FINAL EXAMINATION

CSC258H5S
Computer Organization
Andrew Petersen
Duration - 3 hours
Aids: 1 page(s) of double-sided Letter (8-1/2 x 11) sheet;

The University of Toronto Mississauga and you, as a student, share a commitment to academic integrity. You are reminded that you may be charged with an academic offence for possessing any unauthorized aids during the writing of an exam, including but not limited to any electronic devices with storage, such as cell phones, pagers, personal digital assistants (PDAs), iPods, and MP3 players. Unauthorized calculators and notes are also not permitted. Do not have any of these items in your possession in the area of your desk. Please turn the electronics off and put all unauthorized aids with your belongings at the front of the room before the examination begins. If any of these items are kept with you during the writing of your exam, you may be charged with an academic offence. A typical penalty may cause you to fail the course.

*Please note, you **CANNOT** petition to **re-write** an examination once the exam has begun.*

This final examination consists of 7 questions on 18 pages (including this one). When you receive the signal to start, please make sure that your copy of the examination is complete.

If you need more space for one of your solutions, use the last pages of the exam and indicate clearly the part of your work that should be marked.

Marking Guide

1: _____/ 9
2: _____/ 4
3: _____/ 8
4: _____/ 4
5: _____/12
6: _____/ 5
7: _____/ 8

TOTAL: _____/50

continued on page 2

9 marks **Question 1.** Short Answer

1 mark **Part (a)** Binary Numbers

Provide the 5-bit two's complement representations for the decimal numbers 14 and -14.

1 mark **Part (b)** Binary Arithmetic

Define *overflow* in the context of binary arithmetic.

1 mark **Part (c)** FSMs

What is the key question when deciding between implementing a Moore machine or a Mealy machine?

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3 marks **Part (d)** Compiler Tool Chain

List the major components of the compiler tool chain. For each, describe the input and output and then provide a succinct explanation of the purpose of that component.

CONTINUED ON PAGE 4

1 mark **Part (e)** Pipelining

What is a "control hazard" in the context of pipelining a processor?

2 marks **Part (f)** Pipelining

How does pipelining a processor affect its performance? Consider the impact on both a single instruction and on a stream of instructions.

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4 marks

Question 2. Logic Design

A	B	C	D	Out
0	0	0	0	1
0	0	0	1	0
0	0	1	0	X
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	X
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	X
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

1 mark

Part (a) K-Maps

Use a Karnaugh map to simplify the function described in the truth table above. Provide the k-map and the optimized formula you derive from it.

1 mark

Part (b) Truth Tables

Produce the truth table for a 1-bit full adder. *Recall:* A full-adder has 3 inputs: A, B, and Carry-in (Cin). It has 2 outputs: S and Carry-out (Cout).

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2 marks **Part (c)** Half-Adders and Muxes

Draw the circuit schematic for a 1-bit 2-1 mux that uses **only** 1-bit half-adders and NOT gates. *Recall*: A half-adder has two inputs: A and B. It produces two outputs: S and Carry-out (Cout). *Hint*: Draw a half-adder diagram and a mux diagram using basic logic gates. Then, consider how you can use the gates inside the half-adder to replace the gates in the mux diagram.

CONTINUED ON PAGE 7

8 marks **Question 3.** Storage Devices

2 marks **Part (a)** Latches vs. Flip-flops

What is the key difference between a latch and a flip-flop? Why are flip-flops preferred over latches in almost all applications?

1 mark **Part (b)** Synchronicity

What does it mean for a circuit to be synchronous?

1 mark **Part (c)** SR Latch

Provide the truth table and characteristic question for an (ungated) SR latch.

1 mark **Part (d)** SR Latch

Draw the circuit diagram for a gated SR latch. Use only basic logic gates.

CONTINUED ON PAGE 8

1 mark

Part (e) SR Flip-flop

Using a master-slave configuration, draw the circuit diagram for a positive-edge SR flip-flop. You may use gated SR latches and basic logic gates.

2 marks

Part (f) Register

Draw the circuit diagram for a 1-bit register that takes a *data* input, *clock*, *enable* command, and *reset* command. The device only operates on the positive edge of the clock. *data* is stored if and only if the *enable* signal is high. However, if *reset* is high, the state of the register is set to 0, regardless of the values of *data* and *enable*. You may use SR flip-flops and basic logic gates to build your register.

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4 marks

Question 4. Timing

2 marks

Part (a) Definitions

In the context of circuit analysis, define the following terms:

a. Propagation delay

b. Contamination delay

c. Setup time

d. Hold time

2 marks

Part (b) Delay

The timing analysis we have done in class has not considered *wire delay*: the time required for signals to traverse wires between gates or devices. Wire delay is difficult to predict, so designers are often given a *maximum wire delay* parameter that is the largest amount of wire-related delay that could be added to any path in the circuit.

a. Would wire delay factor into your calculation for the *minimum clock period* of a circuit? If so, how? If not, why not?

b. Would wire delay factor into your analysis of *hold time violations* for a circuit? If so, how? If not, why not?

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12 marks **Question 5.** Machine and Assembly Code

2 marks **Part (a)** Program Execution

What is the role of the program counter (PC) register? Describe how its value can be updated.

3 marks **Part (b)** Machine Code

List the three instruction encodings supported by MIPS. For each, briefly explain the purpose of the encoding.

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1 mark **Part (c)** Function Calls

Why does MIPS separate temporary registers into "caller-saved" and "callee-saved" sets?

3 marks **Part (d)** Exceptions

Explain what occurs when an exception is raised on a MIPS processor. In particular, address *how* the processor identifies the exception to handle and *what* the handler must do to return to normal execution (if it is safe to do so).

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3 marks **Part (e)** Assembly Code

Generate the MIPS assembly for the C-like code below. Define any labels that you need. Assume that `i` is a temporary value that has been assigned register $\$t0$, that `x` is stored in memory at the address indicated by the frame pointer, and that `num` is stored in the global data segment and has a label `num:` that refers to it. If you do not know the exact name of an assembly instruction you wish to use, leave a comment next to the instruction that explains what it should do.

```
for (i = 0; i < num; i++) {
    x = x + i;
}
```

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5 marks **Question 6.** The Memory Model

3 marks **Part (a)** Stack Frames

Draw a diagram that represents the structure of a MIPS stack as defined by Jim Larus. Identify the location of local variables, arguments, and saved registers (naming them when possible), and indicate where the frame pointer and stack pointer should point.

2 marks **Part (b)** Purpose of Segments

Explain what kind of values are stored in each of the following sections of memory.

a. Stack

b. Heap

c. Global Data Segment

d. Text Segment

CONTINUED ON PAGE 14

8 marks **Question 7.** Memory and Caches

2 marks **Part (a)** Associativity

Why might a processor designer choose to implement a 2-way set associative cache over a fully associative cache?

What is the disadvantage of a 2-way set associative cache as compared to a fully associative cache?

2 marks **Part (b)** Locality

Provide definitions for the terms "temporal locality" and "spatial locality" and then explain why programs tend to exhibit both forms of locality.

CONTINUED ON PAGE 15

4 marks

Part (c) Cache Impact

You are part of a team that is building an embedded processor for a specific, well-understood application workload. For the expected workload, 15% of the instructions in the workload are `load` operations, and the cache your team has designed would have an 80% hit rate and a latency of 2 cycles. In contrast, a memory access would take 400 cycles. Unfortunately, your team's manager is concerned about the cost of the cache. Write a well-organized argument for inclusion of the cache that describes the impact of the cache on performance. Provide quantitative evidence for your argument.

Total Marks = 50

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END OF EXAMINATION