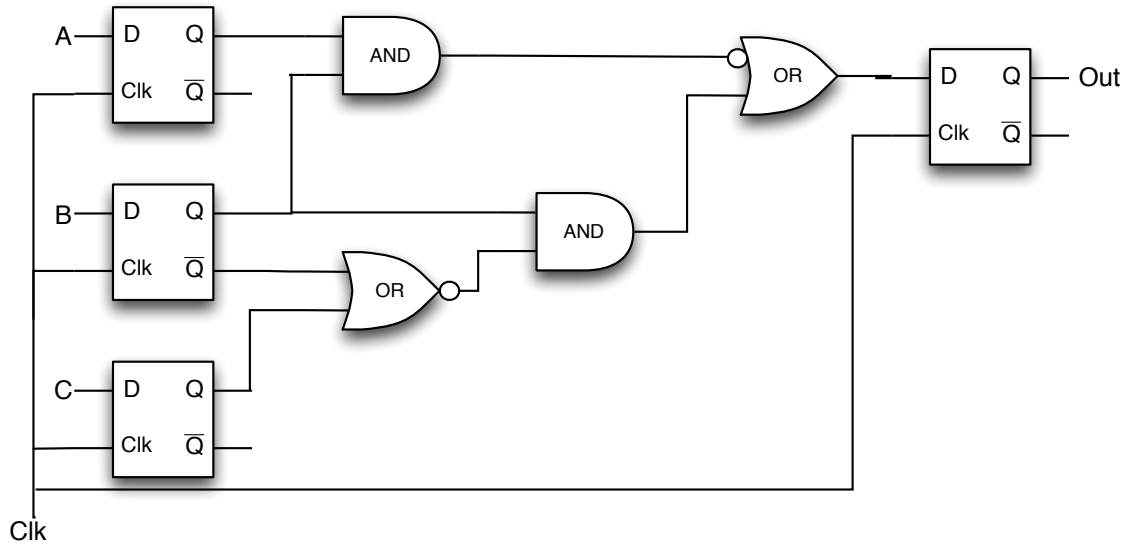
Quiz 1: Ten minutes

1. Define *propagation delay* in a combinational circuit.
2. Given:
   Logical gates: propagation delay of 10, contamination delay of 5
   Flip-flops: setup time of 30, hold time of 15,
   propagation delay of 20, and contamination delay of 7

   What is the total contamination delay of this circuit, including flip-flop delays?

   Please show your work, including identifying the path you will compute.

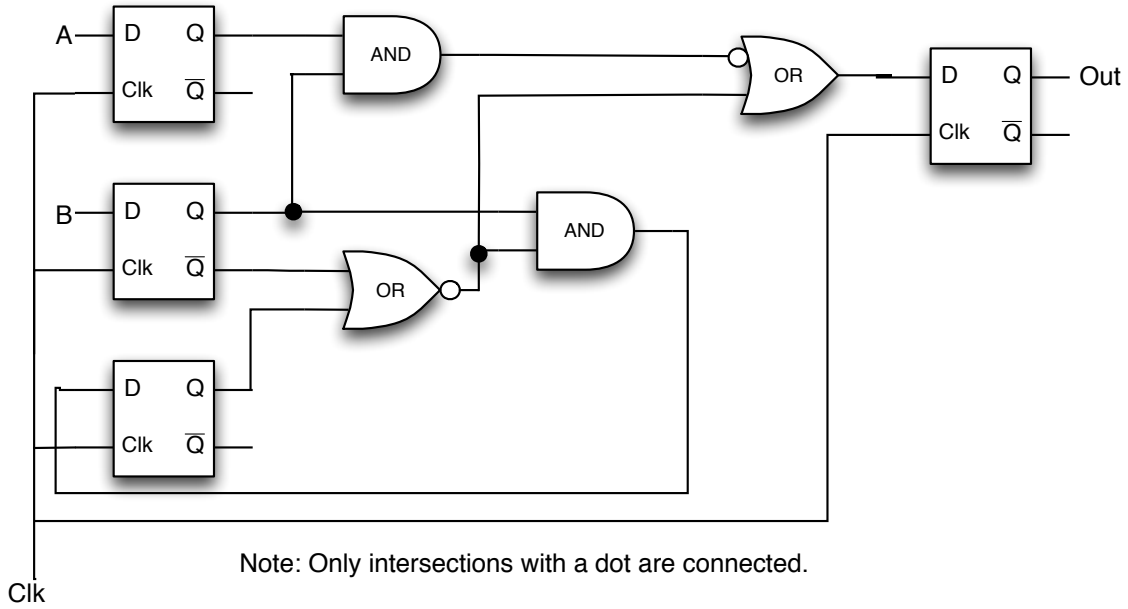


Quiz 1: Ten minutes

1. Define *contamination delay* in a combinational circuit.
2. Given:
   Logical gates: propagation delay of 10, contamination delay of 5
   Flip-flops: setup time of 30, hold time of 15,
   propagation delay of 20, and contamination delay of 7

   What is the total propagation delay of this circuit, including flip-flops delays?

   Please show your work, including identifying the path you will compute.

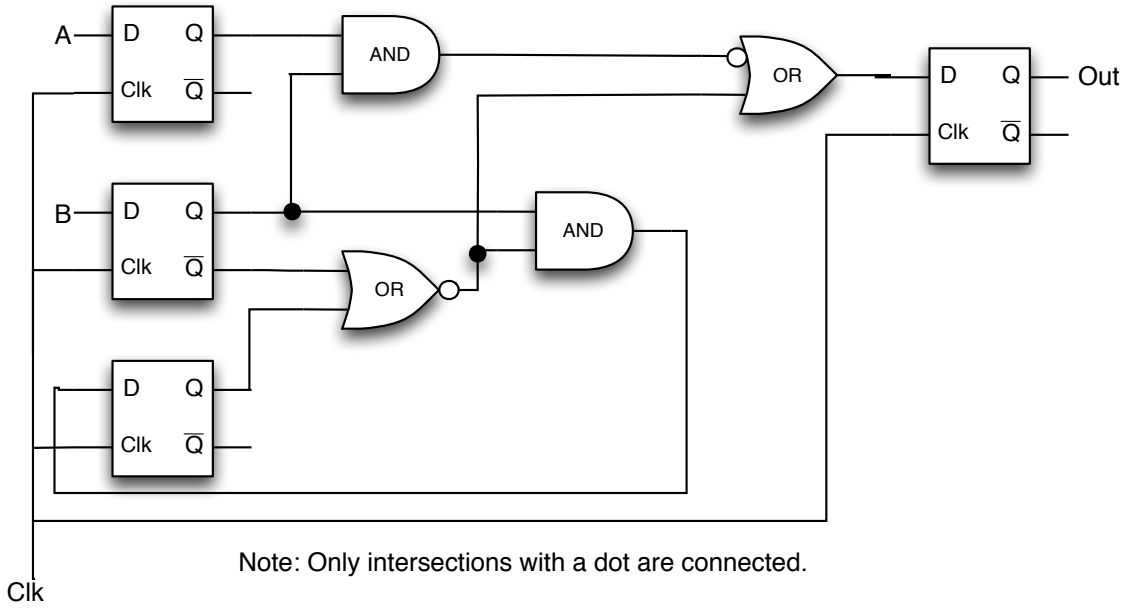


Quiz 1: Ten minutes

1. What is the *setup time constraint* in a sequential circuit?
2. Given:
   Logical gates: propagation delay of 10, contamination delay of 5
   Flip-flops: setup time of 30, hold time of 15,
   propagation delay of 20, and contamination delay of 7

   Is there a hold time violation in this circuit?

   Please justify your answer. If you believe the constraint is violated, identify the path on which the violation occurs.



Quiz 1: Ten minutes

1. What is the *hold time constraint* in a sequential circuit?
2. Given:
   Logical gates: propagation delay of 10, contamination delay of 5
   Flip-flops: setup time of 30, hold time of 15,
   propagation delay of 20, and contamination delay of 7

   What is the total propagation delay of this circuit, including flip-flops delays?

   Please show your work, including identifying the path you will compute.