CSC258: Computer Organization

Latency

Anonymous Feedback

- There are a handful of responses in the thread on the discussion board. Please take a look!

- I've noticed people asking questions or asking for material to be covered …
- Please use the discussion board for that or just talk to me before class.
  - I'm three or four days behind on feedback, so if it's time sensitive, I won't get it until it's too late.

Looking Ahead …

- One more week until reading week.
- This week and next week, the labs will be long. You'll be building a processor.
- This week and next week, we'll cover the last bits of digital design.

Looking Ahead …

- When we get back, the course shifts.
- In lab, we'll do a week of VHDL, and then we'll slide into assembly code.
- In lecture, we'll start talking about *architecture*.

- In essence, the course resets at Reading Week.
- Our job, at the end of the term, is to join the two halves together.

This Week's Lab

- Decoder vs. Demux: A decoder is a general form of a demux. You can use one to build a demux.
- Register design: A register is a multi-bit storage device. Our register is a *parallel* device.
- Buses: When building multi-bit devices, you'll want to use the bus tool to bundle wires together.

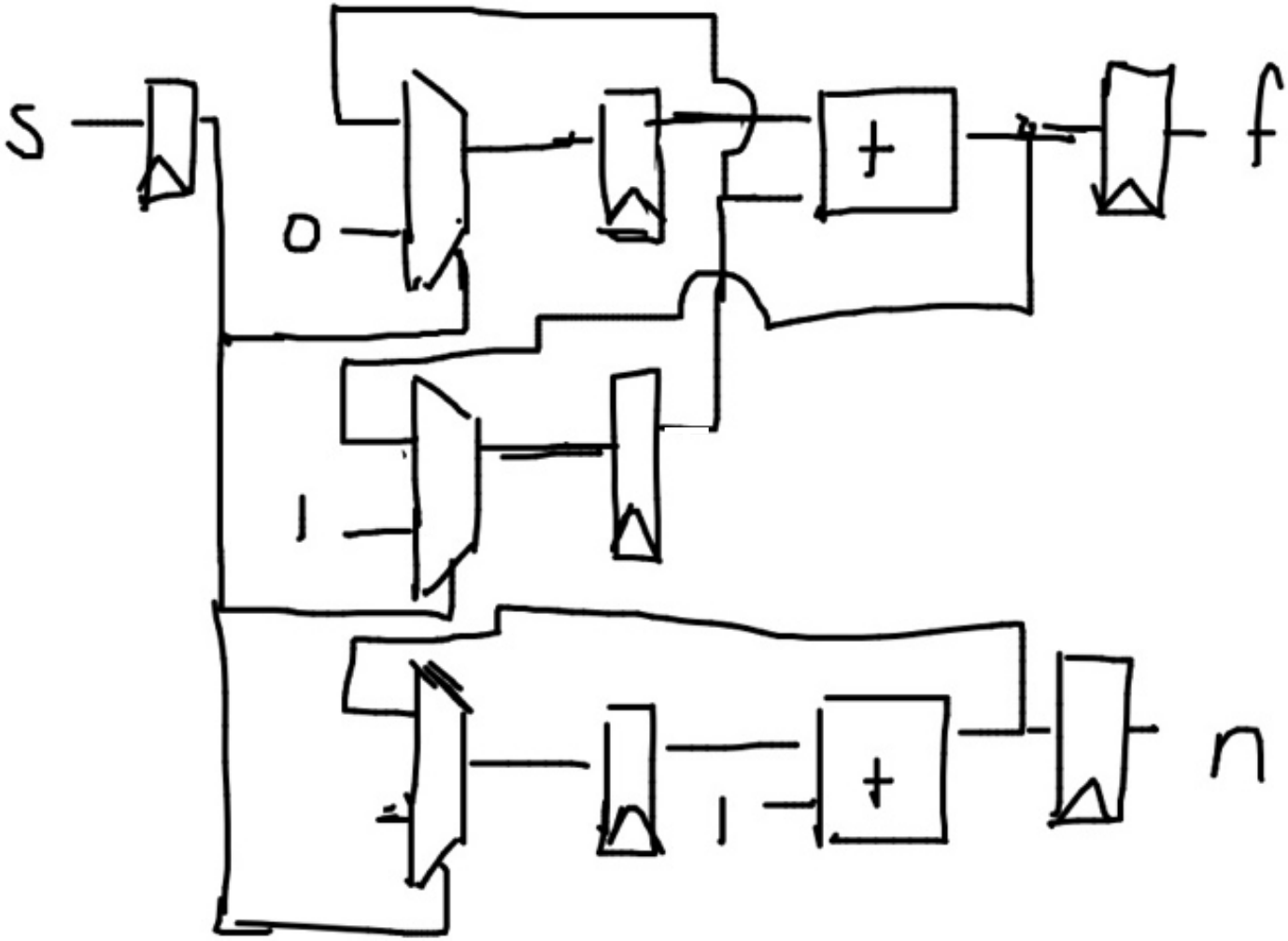
- This lab will take some time to complete. Next week's lab will take that into account, and you will have a chance to catch up over reading week.

Latency

Terms

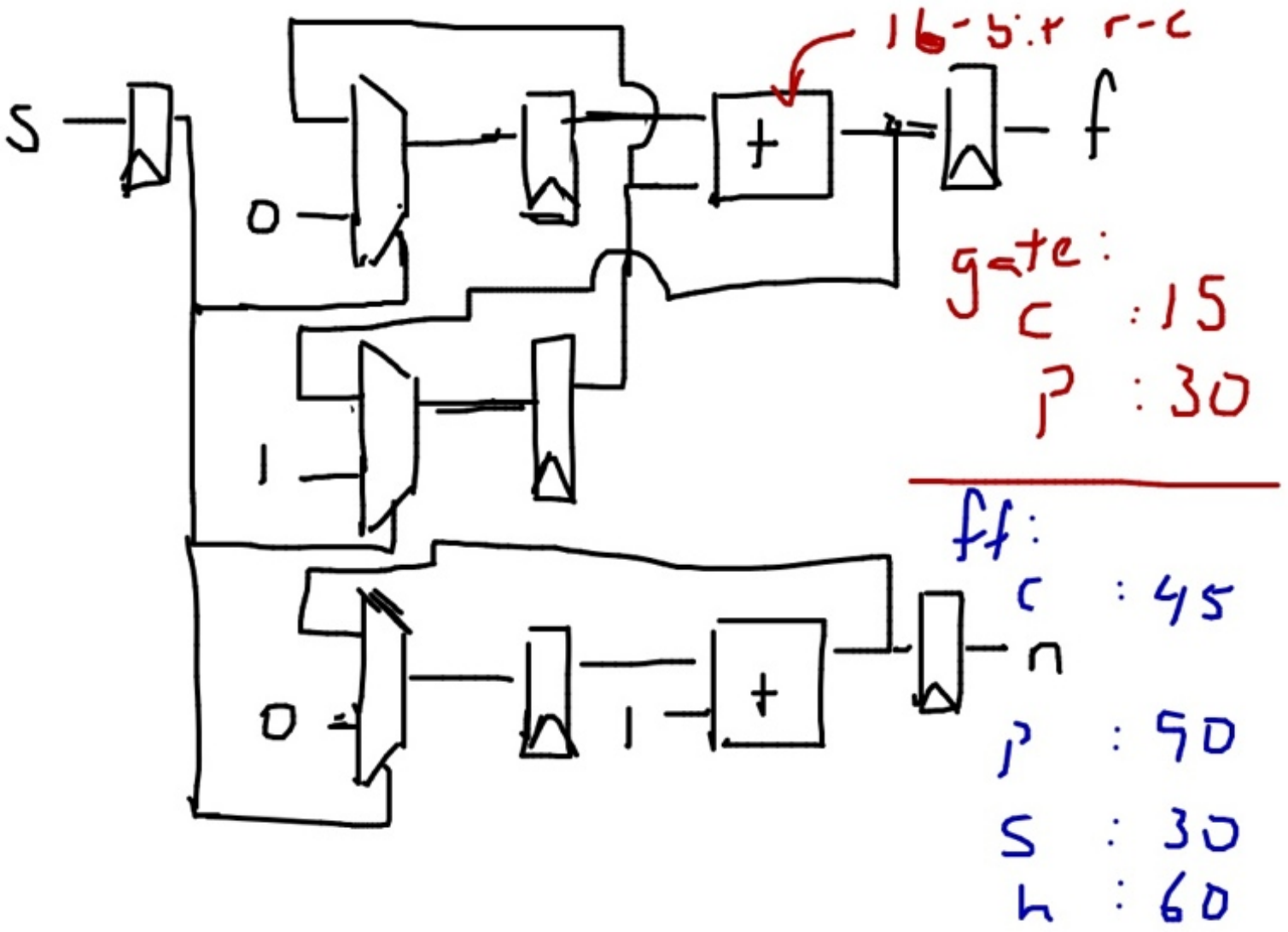
- *Contamination delay* -- minimum time until the output becomes unstable
- *Propagation delay* -- maximum time necessary to get the correct answer from a device after the inputs are provided.
- *Setup time* -- time before the clock is received before which the inputs must have arrived.
- *Hold time* -- time after the clock signal is received during which the inputs must be stable.

Example Circuit

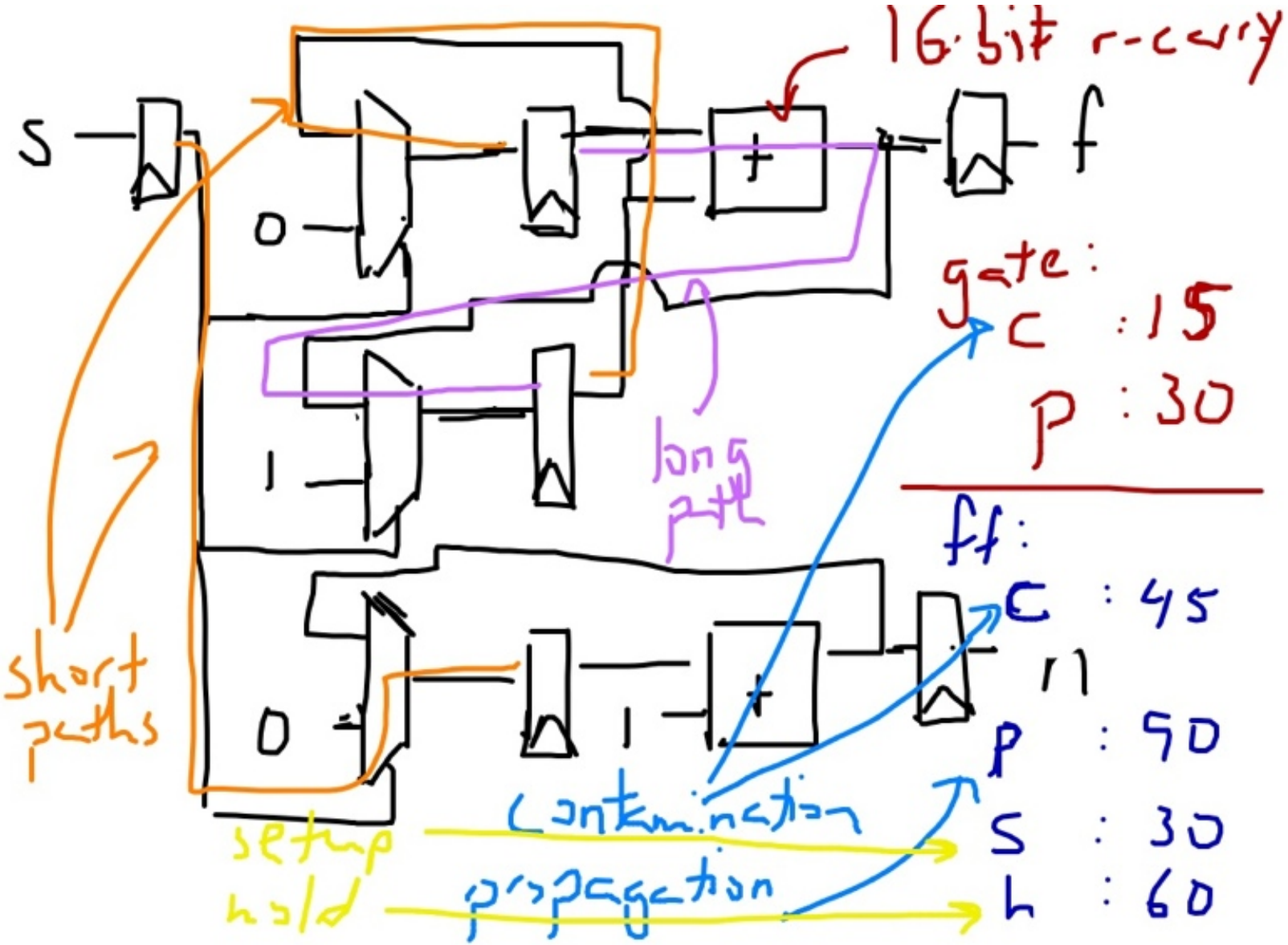


What does this circuit compute?

Adding Delay Parameters



Identifying Candidate Long and Short Paths

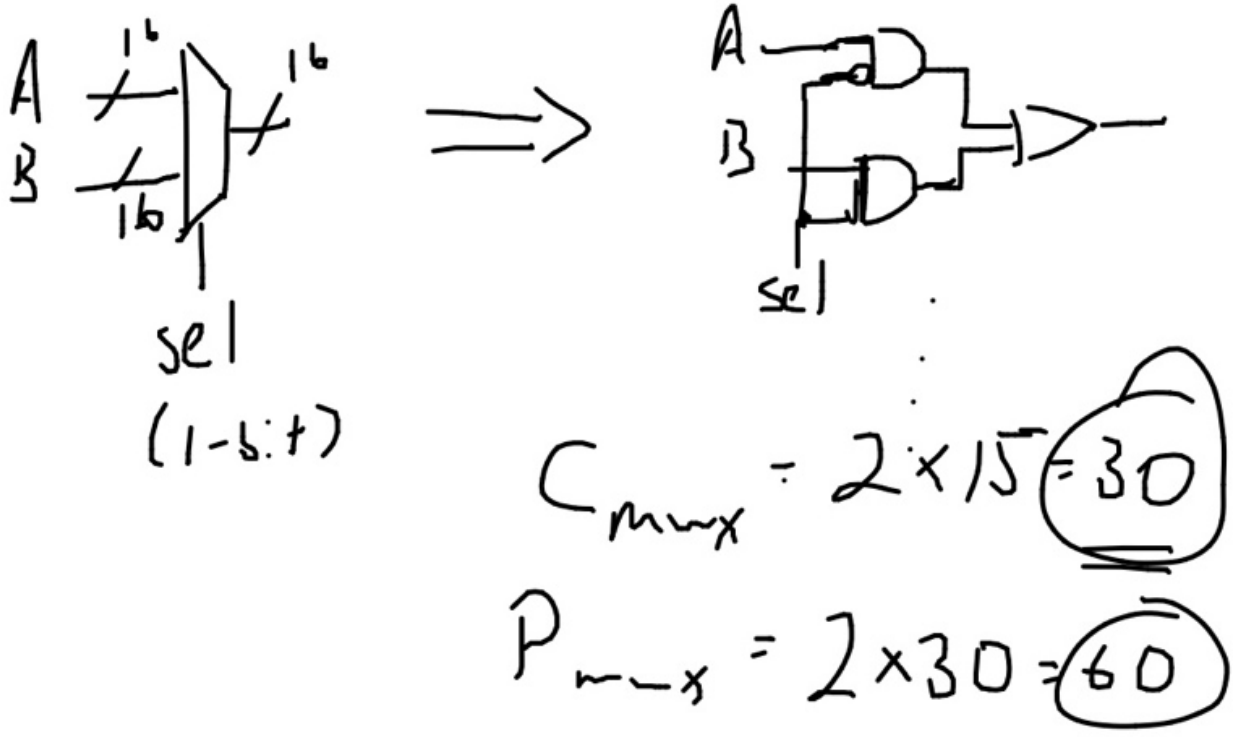


Propagation Delay

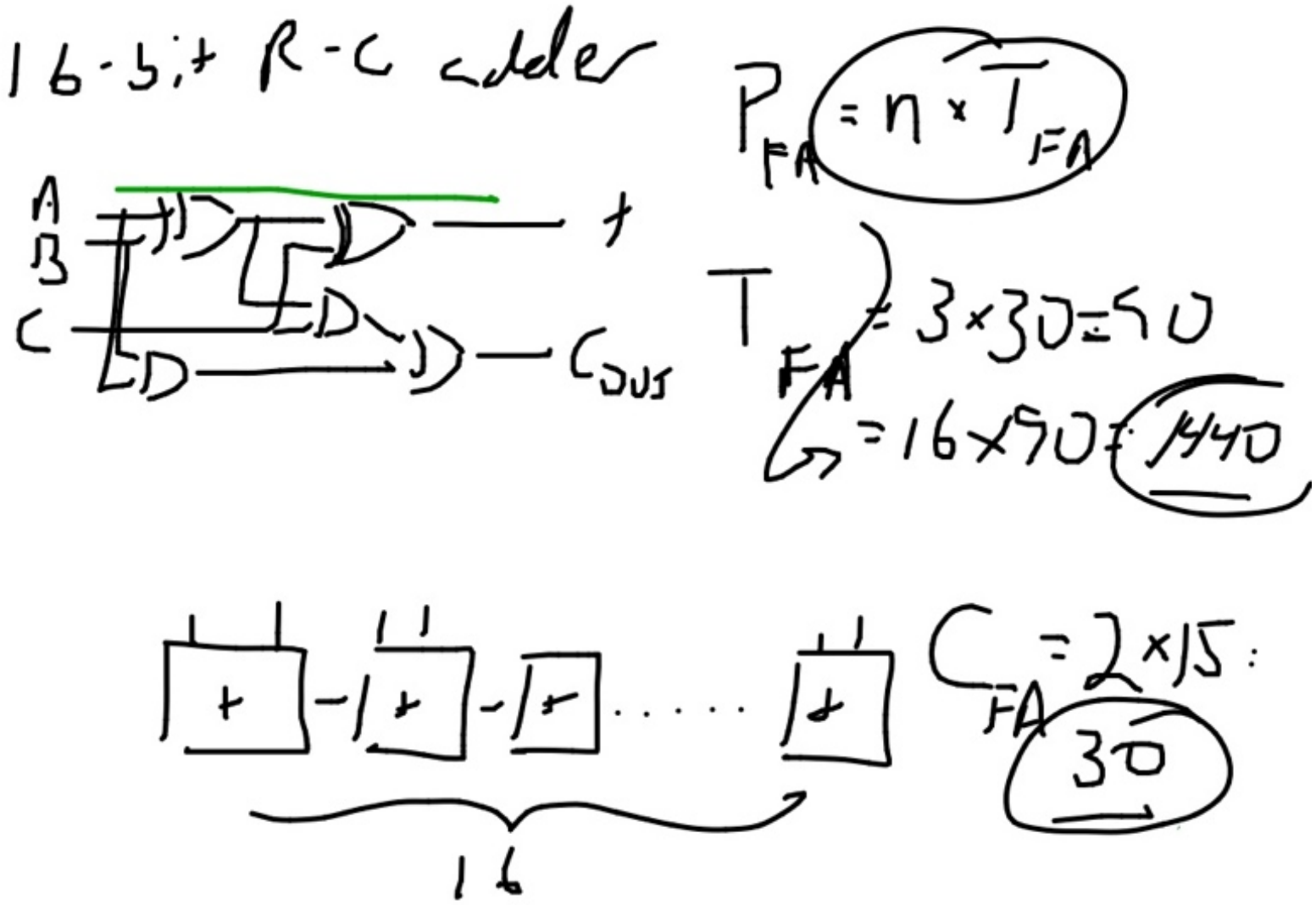
- The longest path through the circuit determines the maximum legal clock frequency.

- Find a longest path, then calculate the sum of all of the maximum delays on that path. In our case:
  - Propagation delay on a FF (90 units)
  - Propagation delay on an adder *(must calculate!)*
  - Propagation delay on a mux *(must calculate!)*
  - Setup time on a FF (30 units)

Calculating Contamination and Delay Values for the Muxes



Ripple Carry Delay:
Next Week's Reading

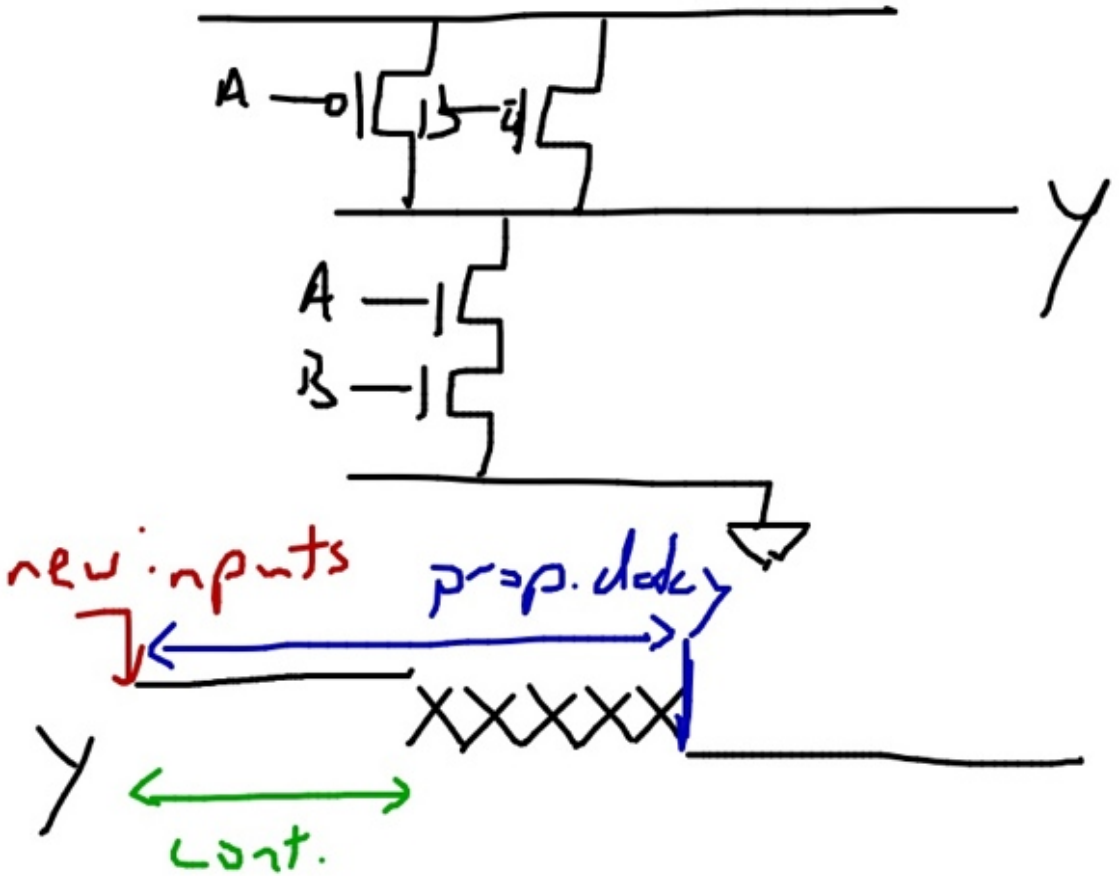


Ripple Carry

- Can we do better than 1440?
- What if we looked inside the devices?

- Hint: The long path for all of the adders except for the first is actually from C to Cout. (Why?)

Why are Contamination and Propagation Delay Different?



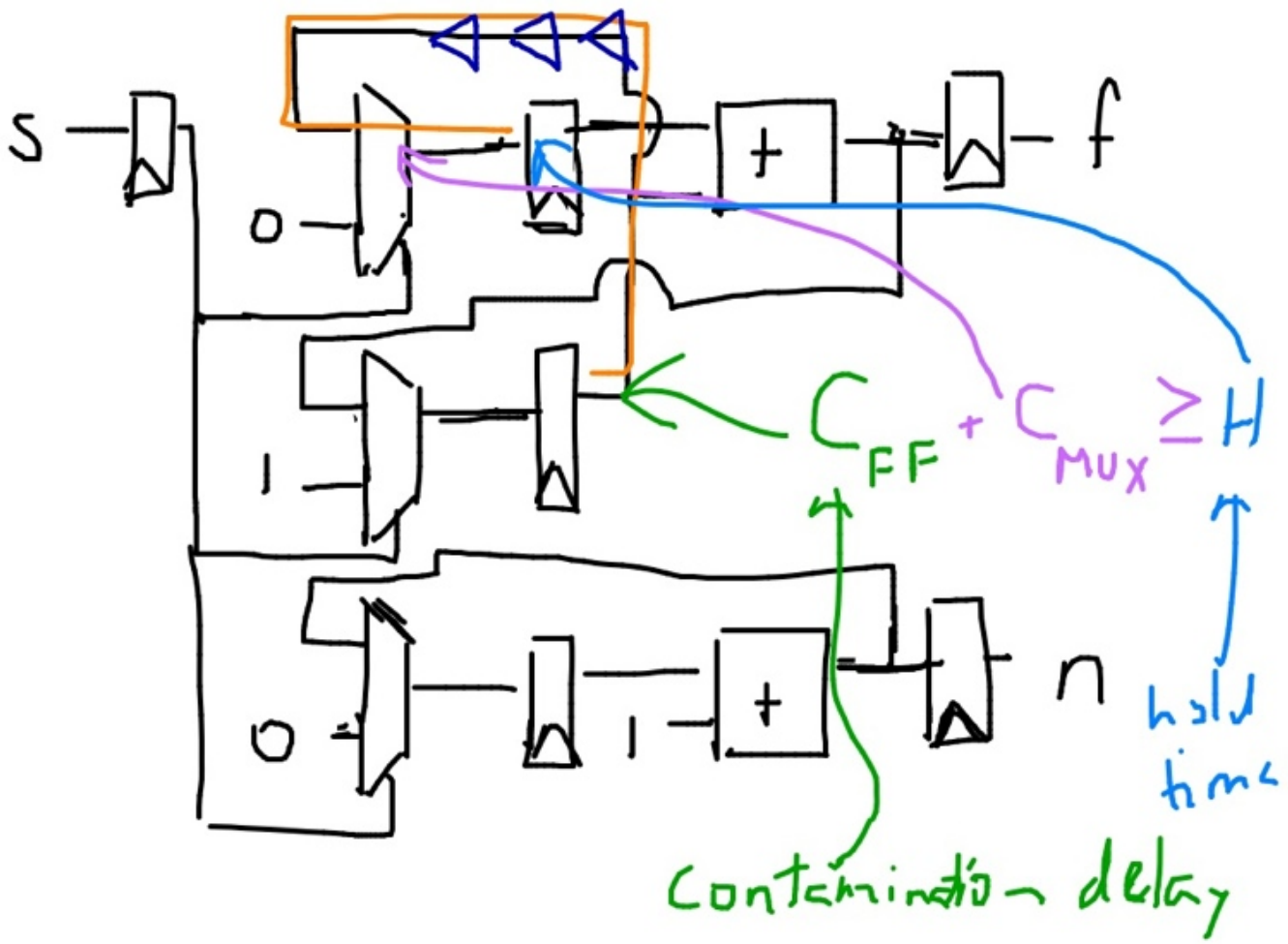
1. There are multiple paths through a gate.
2. Transistors change value quickly -- but not instantaneously.

These factors lead to unstable output values.

Contamination Delays

- Propagation delays are used to calculate the maximum time required before the answer is available.
- In contrast, contamination delays are used to find the shortest path.
  - If a path is too short, then the hold time of the flip-flop storing the output may be violated.

Hold Time Constraint



If the hold time constraint is violated, buffers can be added to increase the contamination delay on the path.