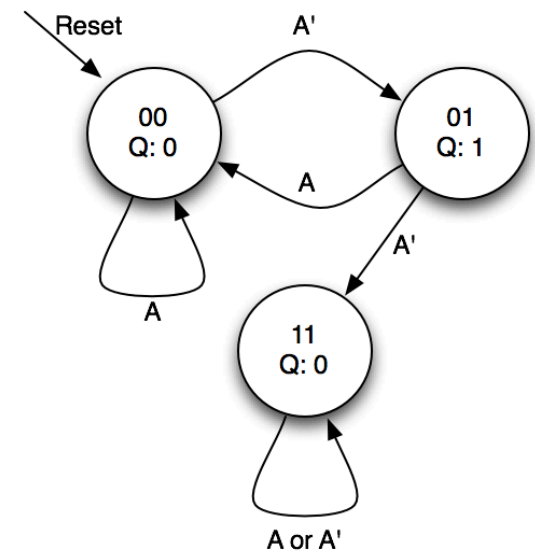# Quiz 1: Ten minutes

1. Draw the *state transition diagram* for a Moore machine that takes an input A, and outputs 1 if and only if the number of clock cycles where A has been high (had value 1) is a multiple of three.

2. Please provide a definition or an example of the term *race condition*.

Quiz 1: Ten minutes

1. What is a *synchronous sequential circuit*?

2. You are designing an elevator controller for a building with 40 floors. The controller has two inputs: *UP* and *DOWN*. It produces an output indicating the floor that the elevator is on. What is the minimum number of bits required to store the controller's state? (Please justify your answer.)

3. Is a counter a finite state machine? Please justify your answer.

Quiz 1: Ten minutes

1. Is the state diagram to thee right describing a Mealy Machine or a Moore Machine? Explain why.

2. Complete the state transition table and output table for the FSM to the right.

Reset

A'

00
Q: 0

01
Q: 1

A

A

A'

11
Q: 0

A or A'

Note: ' designates "not"