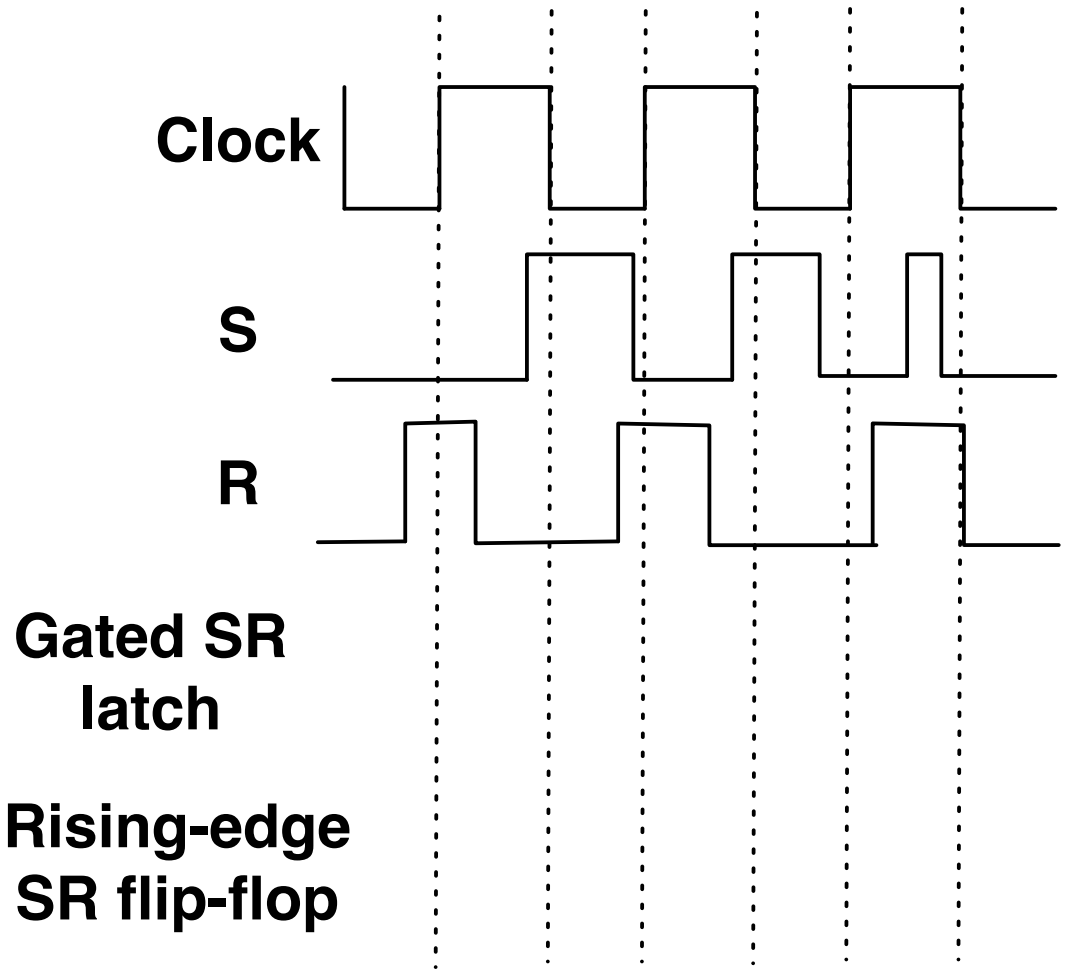
2 marks **Part (d)** Timing

Given the input waveform below, sketch the output, Q, of an SR latch and SR flip-flop.



2 marks **Part (e)** FSMs and Processors

Explain how the MIPS processor in the textbook is a finite state machine.

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