Question 3. Sequential Circuits [5 MARKS]

In this problem, you will be exploring the design of a FSM with three inputs – A, *reset*, and a *clock* – and one output – *majority*

majority should be 1 if the majority of the last three inputs A have been 1. Whenever a *reset* is received, regardless of the *clock*, the FSM is reset to a starting state where no A inputs have been recorded. (Note: A circuit that calculates 1 if and only if a majority of its inputs are 1 (a "majority" circuit) will be very useful; what does it look like?)

Part (a) [2 MARKS] Draw the Mealy state-machine diagram for this FSM. Label each state with its binary representation. (Recall: Mealy machines provide output based on the current state and the new input, so label each edge with the input it represents and any outputs that should be 1.)

Part (b) [1 MARK] Briefly explain how the *clock* input is used in this circuit. (i.e. What does it mean for "the last three inputs A (to) have been 1?")

Part (c) [1 MARK] Describe the device(s) you will use to store the state.

Part (d) [1 MARK] Sketch the schematic for this FSM. You may use the sequential device you have described in the previous subquestion and any basic logic gates you need.