Question 3.

8 marks

Finite State Machines

Design a circuit to recognize the language $(RS^*R+)+$. Your circuit should take 3 1-bit inputs (R, S, and reset) as well as a clock signal. Exactly one of the three inputs will be high at the positive-edge of the clock; the input that is high is the "value" of that cycle. Output a 1-bit Valid signal. Valid should be high if the sequence of values received since the last reset is a member of the specified language and low otherwise.

Provide your state diagram with transitions clearly labeled, truth tables for "next_state" and "Valid", and a circuit schematic. You may use any component we have discussed in class in your design (registers, muxes/demuxes, logic gates, etc.). If you use a high-level component like a register, please clearly label its inputs and outputs.