University of Toronto Mississauga

Midterm Test

Course: CSC258H5 Winter 2019

Instructor: Larry Zhang

Duration: 90 minutes

Aids allowed: None

Last Name: _____

Given Name: _____

Flip to the back cover and write down your name and student number.

This midterm consists of a total of 67 marks, for 6 questions on 14 pages (including this one). When you receive the signal to start, please make sure that your copy is complete.

Each question is labelled with the suggested amount of time that you should spend on it. You may use it as a reference to better manage your time.

Precise answers will be given higher marks than vague ones. Concise answers will be given higher marks than lengthy ones. Illegible answers will not be given marks. If you write an answer on one of the blank pages, indicate clearly what you want to be marked.

You know more than you think you do!

Question 1: Very Short Answers [2x10=20 marks] [15 minutes]

For multiple choice questions, a mark will be deducted for both missing choices and wrong choices.

1. After doping silicon with phosphorus, which of the following is true? Circle all that apply.

    a. the material becomes negatively charged

    b. the material becomes positively charged

    c. the material has positive free charge carriers

    d. the material has negative free charge carriers

2. Assuming 4 inputs A, B, C and D, which minterm is **A'BC'D**? Write down the **decimal** number in the blank below.

m_____

3. Assuming 4 inputs A, B, C and D, which maxterm is **A' + B + C + D**? Write down the **decimal** number in the blank below.

M_____

4. Consider the 6-bit signed binary number **111010**. Write down its **decimal** value in the space below.

5. Consider the following subtraction between two signed numbers **(110010 - 010101)**. Write down its result as a **6-bit binary number** in the space below.

6. How many **selection bits** are needed at least to implement a 258-to-1 mux?

7. Assuming two inputs A and B, and given the Sum-of-Minterms **AB' + A'B' + AB**, write down the equivalent **Product-of-Maxterms** in the space below.

8. What is the logical expression of the **sum bit S** of a **full adder** in terms of inputs **X, Y,** and **Cin**?

S = _____

9. Consider a finite state machine with 84 states. Which of the following is true? Circle all that apply.

   a. we need at most 7 flip-flops to implement this FSM

   b. we need at least 7 flip-flops to implement this FSM

   c. It is possible to use 6 flip-flops to implement this FSM

   d. It is possible to use 8 flip-flops to implement this FSM

10. Below are four circuits with inputs **A, B** and output **Y**. Three of them are equivalent to one another. Circle the one that is **different** from the other three.
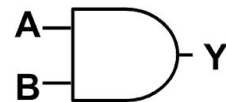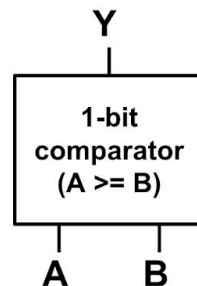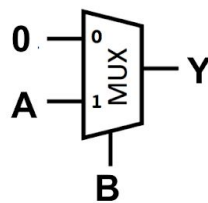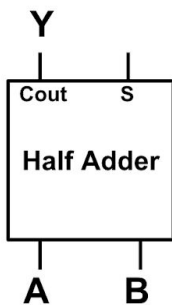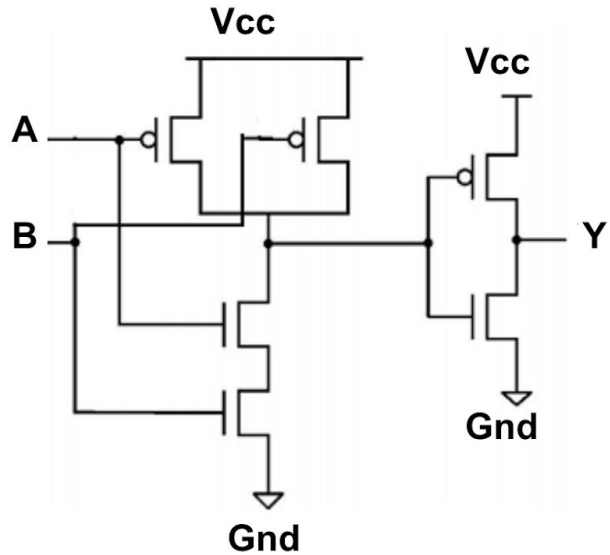
Question 2: Short Answers [16 marks] [20 minutes]

1. Consider the following two MOSFET circuit diagrams. In the blanks below, write the logical expressions of the output Y in terms of the inputs A and B. [4 marks]
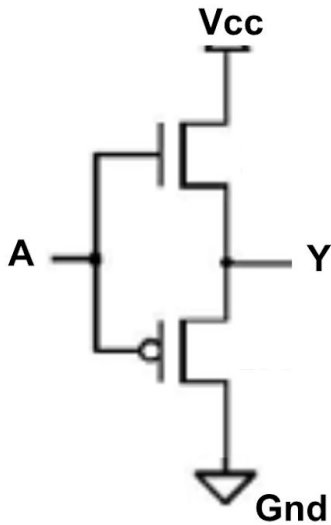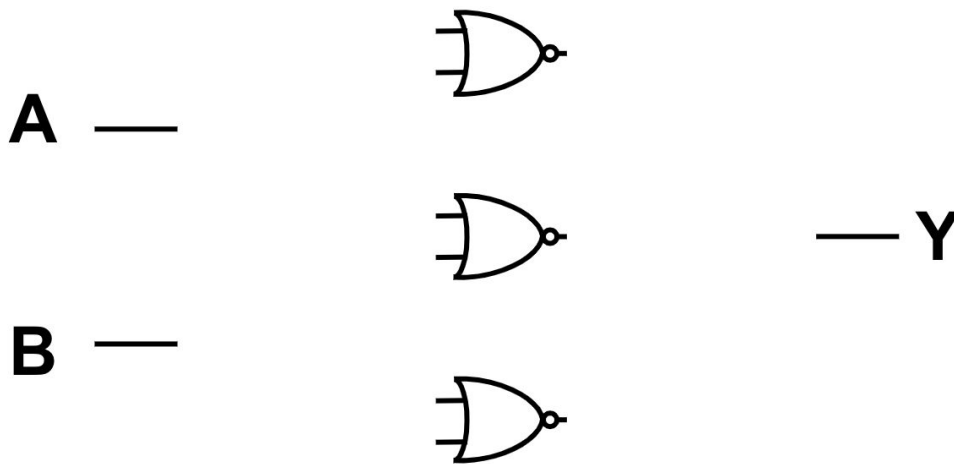

Y = _____

Y = _____

2. Below, complete the circuit diagram of a **2-input AND** logic using three instances of **NOR** gates, i.e, make it so that **Y = A and B**. You are **only** allowed to add **wire** to the diagram, i.e, you're NOT allowed to add any other logic gate or any constant input value (0 or 1). [4 marks]

3. Consider the following sequential circuit with three D flip-flops and two XOR gates. Assume that **X = 1** all the time, and that initially at time **t = 0**, the value of the flip-flops are **Q2 = Q2 = Q0 = 0**. In the table below, write the values of **Q2, Q1, Q0 and Y** at time **t = 1** (after one clock cycle) and **t = 2** (after two clock cycles). [4 marks]
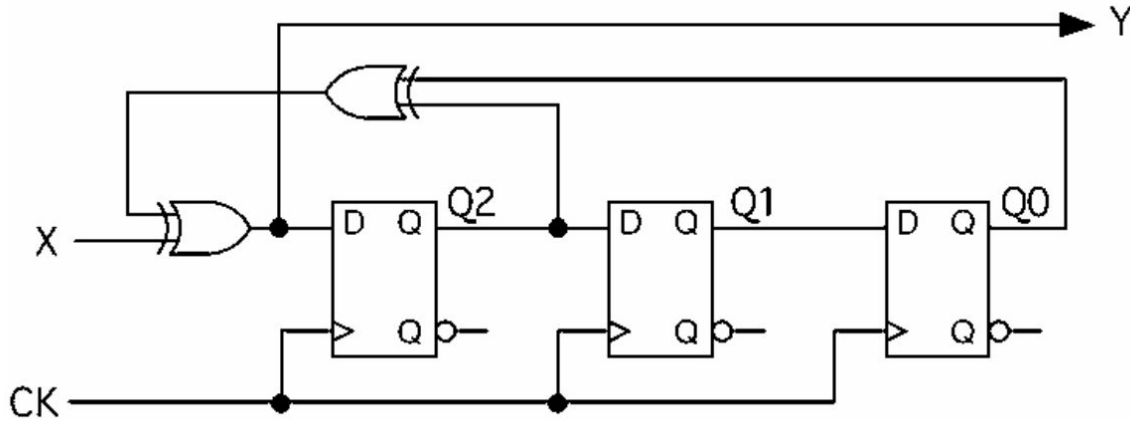
	Q2	Q1	Q0	Y
t = 0	0	0	0	1
t = 1				
t = 2				

4. Consider the following latch-like circuit which uses both NAND and NOR gates. On the right side, you are provided with a sequence of changes of the inputs A and B. By filling in the blanks, you will write the output values P and Q for each step of the changes. For each blank, the value you fill in could be one of the following: **0, 1,** or **X** (indeterminate value). [4 marks]
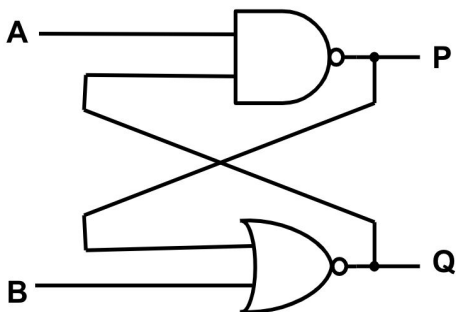
Initially, A = 0, B = 0, now P = _____ , Q = _____

then flip B, i.e., A = 0, B = 1, now P = _____ , Q = _____

then flip A, i.e., A = 1, B = 1, now P = _____ , Q = _____

then flip B, i.e, A = 1, B = 0, now P = _____ , Q = _____

Question 3: Combinational Design [8 marks] [8 minutes]

You'll get 1 out of 8 marks for leaving this question completely blank.

We would like to implement a combinational circuit with four inputs A, B, C, D and one output Y with the following behaviour: the output Y is 1 if and only if the binary number ABCD is a **multiple of 3** (note that zero is a multiple of 3); and the input value ABCD can **ONLY** be in the range from 0 to 9, i.e., the value of ABCD will **NEVER** be greater than or equal to 10 (ten). Complete the design of this circuit by answering the following questions.

(a) Below, complete the K-map of the circuit by filling in the cells with correct values according to the above specification of the circuit. [4 marks]

	AB	A'B	A'B'	AB'
C'D'				
C'D				
CD				
CD'				

(b) Draw the optimal set of boxes on the above K-map and write below the simplified logical expression of the output Y. Full marks will only be given to a correct optimal logical expression based on the correct K-map from Part (a), so please first make sure your answer to Part (a) is correct. [4 marks]
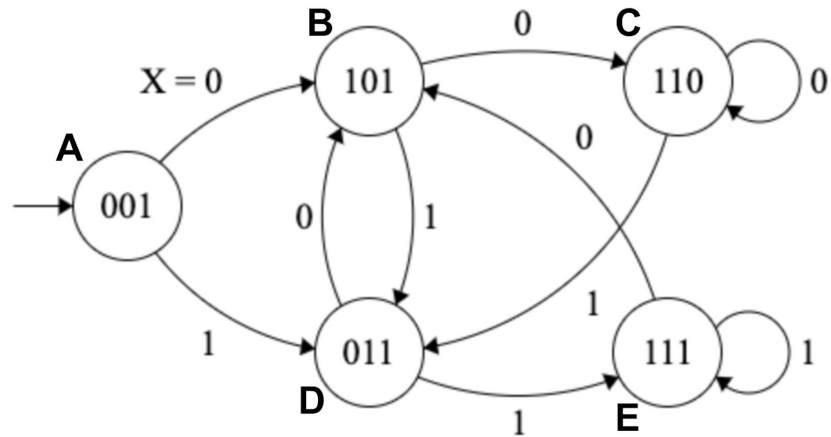
Y = _____

[This blank page will not be marked unless you clearly indicate the part that should be marked.]

Question 4: Finite State Machine [7 marks] [8 minutes]

You'll get 1 out of 7 marks for leaving this question completely blank.

Consider a circuit that implements the following finite state machine with five states A, B, C, D and E. The binary value displayed in each circle represents the flip-flop values that are assigned to the state, in the order of **F2 F1 F0.** For example, State A with value 001 means that the assigned flip-flop values are F2 = 0, F1 = 0, F0 = 1. The input of the circuit (in addition to the clock input) is named **X** (the value read on each transition) and the output of the circuit is named **Y**. Assume that the circuit is in State A initially.

(a) Let the output of the circuit be **Y = F1 and F2**. Below, by filling in the blank, describe what this circuit does. The description must be as concise as possible. [3 marks]

The output Y is high if and only if _____

(b) Identify **four** transitions in the above FSM that could cause unexpected behaviour. Write the transitions by filling in the blanks below like this: "A → B". [4 marks]

#1: _____ → _____

#2: _____ → _____

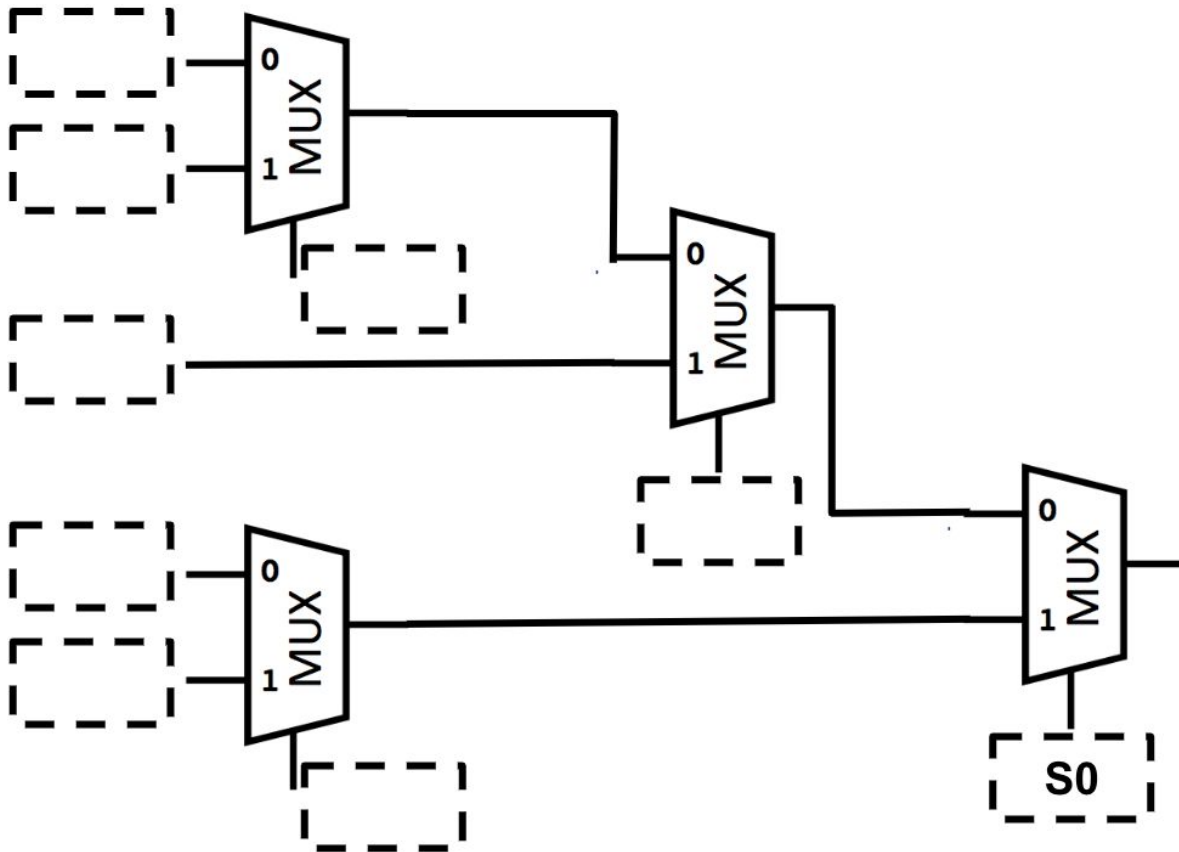**#3:** _____ → _____

#4: _____ → _____

[This blank page will not be marked unless you clearly indicate the part that should be marked.]

Question 5: Multiplexers [8 marks] [8 minutes]

You'll get 1 out of 8 marks for leaving this question completely blank.

Below is the circuit of a 5-to-1 multiplexer (mux). It has 5 bits for data input (**D0, D1, D2, D3, D4**) and 3 bits for the selection input (**S2, S1, S0**). The 5-to-1 mux is expected to work in such a way that the value of the selection input combination directly reflects the data input being selected, i.e., (S2, S1, S0) = (0, 0, 0) selects D0 as the output, (S2, S1, S0) = (0, 0, 1) selects D1, (S2, S1, S0) = (0, 1, 0) selects D2, (S2, S1, S0) = (0, 1, 1) selects D3, and (S2, S1, S0) = (1, 0, 0) selects D4. We don't care about the output when (S2, S1, S0) is (1, 0, 1), (1, 1, 0) or (1, 1, 1).

Fill in the blank boxes in the circuit below with input names (S0, S1, S2, D0, D1, D2, D3, D4) so that the 5-to-1 mux works as specified above. One of the boxes is already filled in for you.

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Question 6: Counters [8 marks] [15 minutes]

You'll get 1 out of 8 marks for leaving this question completely blank.

(a) Below, complete the circuit of a 2-bit **asynchronous DOWN counter**, i.e., upon each clock cycle, the value represented by **Y1Y0** changes like 0, 3, 2, 1, 0, 3, 2, 1, 0, etc. You are ONLY allowed to add **wires** and **constant input values** (such as 1 or 0) to the circuit; you are **NOT** allowed to use **any** logic gates such as AND gate, OR gate, NOT gate and XOR gate. [4 marks]
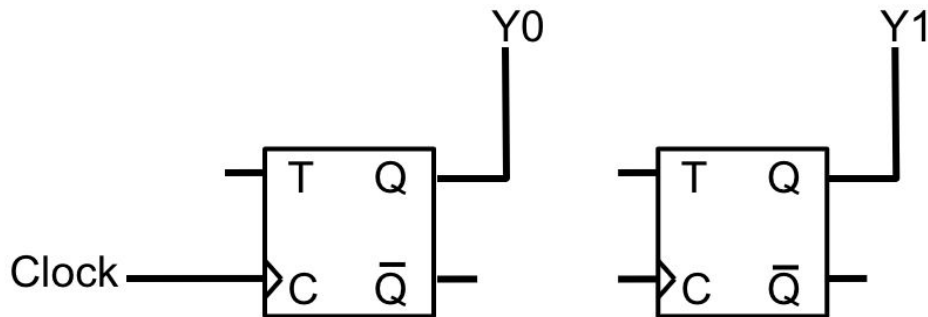
(b) Below, complete the circuit of a 2-bit **synchronous 0-to-2 counter**, i.e., upon each clock cycle, the value represented by **Y1Y0** changes like 0, 1, 2, 0, 1, 2, 0, 1, 2, 0, etc. You are ONLY allowed to add wires, constant input values (such as 1 or 0), and **at most one instance** of **AND** gate or **OR** gate, i.e., you're NOT allowed to use more than one logic gates, and you're NOT allowed to use any logic gate other than AND and OR. [4 marks]
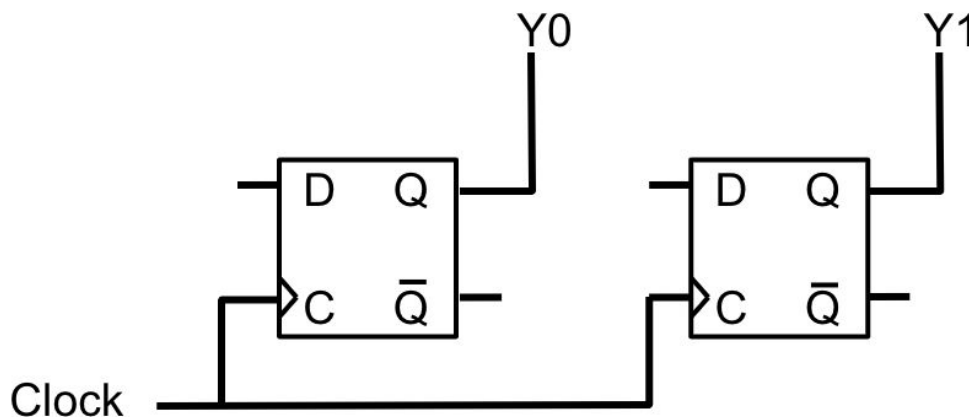
[This blank page will not be marked unless you clearly indicate the part that should be marked.]

Last Name: _____

Given Name: _____

Student Number: _____

Q1: _____ / 20

Q2: _____ / 16

Q3: _____ / 8

Q4: _____ / 7

Q5: _____ / 8

Q6: _____ / 8

TOTAL: _____ / 67

END OF TEST