

CSC258H Lab 4: Sequential Logic

1 Introduction

This week, we'll examine the behavior of circuits which maintain internal state. These circuits are called latches and flip-flops. Designs which utilize these circuits are called “sequential”, since data proceeds through them in a linear fashion with latches and flip-flops used to break the design into stages.

Required Submissions: This lab requires the submission of a circuit file (“lab4.circ”) and a lab report (“lab4report.pdf”) to MarkUs by **Tuesday, February 9, 10:00 PM**. Please read the syllabus regarding the late policy. All submitted work must be completed **individually**.

2 SR Latches

In your lab report, write down the truth table for a gated SR latch like the one below. How many columns of input does your table have? Clearly, it should have columns for S and R. What about the Clock? How about the internal state (the initial values of Q and NotQ)? How many rows does the table have? How many circuit state and input combinations do you need to test to fully verify the circuit?

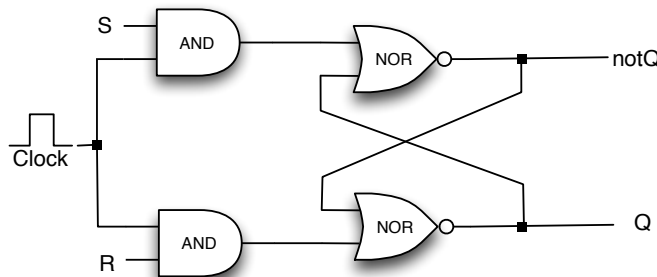


Figure 1: A gated SR latch

Use a Logisim-Evolution circuit to implement the gated SR latch above. Include three input pins as input to the circuit instead of connecting the clock input to a clock component (so that later you can reuse this circuit as a symbol). During testing, we will want to control when clock pulses arrive, and using a third input for the clock input gives us the flexibility to connect that input to a device like a switch or push button.

Using your truth table, test your circuit. Does the output of the circuit match your truth table? Can you use an example to explain why the gated SR latch is NOT edge-triggered?

3 D Flip-flop

The output of a latch changes whenever the clock input is high – during the positive “pulse”. In contrast, the output of a flip-flop only changes when the clock input is changing. Typically, we build positive edge flip-flops – ones that change when the clock input changes from low to high. We could

implement latches that change when the clock input is low (negative pulse), and similarly, a flip-flop could be implemented to change on the negative edge. The latter would be called a “negative-edge triggered flip-flop” or “falling-edge triggered flip-flop”.

A D latch is very similar to an SR latch, except that, in a D latch, the S and R signals are always negations of each other (refer to the lecture slides for more details). A master-slave D flip-flop is a series of two D latches which have opposite clock signals (refer to the lecture slides for more details).

In the lab, create a separate circuit and use the SR latch from the last section to implement a D latch, which is a slight modification to the gated SR latch. Then, create another circuit and use two D-latches to implement the **positive-edge** triggered D flip-flop. Your design should take two inputs – D and Clock. It should produce a single output Q. Test your circuit to verify that your design works as expected. Demonstrate the circuit to the TA and convince them that your D flip-flop is edge-triggered rather than pulse-triggered.

4 Lab Report

Include the following in your lab report named “lab4report.pdf”.

- Your name and student number.
- The truth table for the gated SR latch.
- The circuit diagram of your D-latch.
- The circuit diagram of your D flip-flop, using symbols of the D-latch.
- A waveform diagram, along with a short explanation, demonstrating that your gated SR latch is pulse-triggered.
- A waveform diagram, along with a short explanation, demonstrating that your D flip-flop is edge-triggered.

(You may generate the waveforms using any tool you like. Hand-drawing is also OK as long as it is clear.)

5 Summary of TODOs

Below is a short summary of the steps to be completed for this lab:

1. Before the lab, read through the lab handout. Write down the truth table of the gated SR latch.
2. In the lab, create `lab4.circ`, implement the gated SR latch, test the circuit to fully verify the truth table that you created. Demonstrate the circuit to the TA that your SR latch is pulse-triggered.
3. Use your gated SR latch circuit to build a D latch circuit.
4. Use your D latch circuit to build a D flip-flop circuit.

5. Test the D flip-flop. Convince your TA that your flip-flop is edge-triggered rather than pulse triggered.
6. Complete the lab report.
7. Submit `lab4.circ` and `lab4report.pdf` to MarkUs before the deadline.

Evaluation (2 marks in total):

- 0.5 mark for the truth table of the gated SR latch
- 0.5 mark for the circuit diagrams of the D-latch and the D flip-flop
- 1 mark for the waveforms and explanations.