CSC258H Lab 2: Circuit Creation

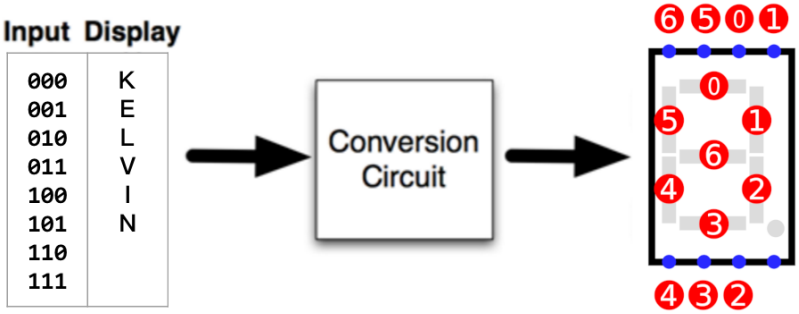
1 Introduction

This week, we'll practice designing circuits made of logic gates using Karnaugh maps. You'll need to be familiar with the software tools we used last week; refer back to last week's lab if you need to refresh your memory.

Required Submissions: This lab requires the submission of a circuit file ("`lab2.circ`") and a lab report ("`lab2report.pdf`") to MarkUs by **Tuesday, January 26, 10:00 PM**. Please read the syllabus regarding the late policy. All submitted work must be completed **individually**.

2 Driving a 7-Segment Display

A 7-segment display takes a 7-bit number as input. The figure below is the 7 segment display in Logisim-Evolution; the number on each segment refers to index of the bit that determines whether it is lit ("on") or dark ("off").

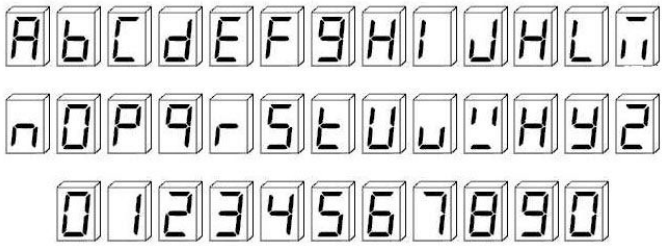


We would like a circuit that can be used to greet your TA on the 7 segment display. Since the lengths of messages will be 8 letters (including the space), the circuit needs three input bits. The figure above also shows an example how the inputs could match to the letters. In the example, the input `000` should display the letter `K`. Therefore, the circuit you will design should produce the 7-bit output `1110110`. You may, if you wish, rearrange the assignment of letters to inputs to create a simpler circuit.

Below are the messages that you need to show depending on the lab section you are enrolled in. Note that you must also properly display the space character, i.e., all segments should be off when you switch to the space.

Tutorial Section	Message
PRA0101	`HEY NIVY`
PRA0102	`SUP NORA`
PRA0103	`HI ARMIN`
PRA0104	`YO KEVIN`
PRA0105	`SHAR VEN`
PRA0106	`TY ARMIN`
PRA0107	`YEP ARSH`
PRA0108	`O HASEEB`
PRA0109	`LEO NARD`
PRA0110	`BYE NORA`
PRA0111	`MARCO EH`

Below is a picture that shows how each English letter should be displayed on the 7-segment display.



First, **before the lab**, generate the expressions for the seven optimized circuits – one for each output (segment on the display). To do so, you'll need to create a truth-table with 3 input bits and 7 output bits. Then, you should use seven K-maps – one for each output – to generate the optimal logic expression that expresses it.

Once you arrive in lab, create a new Logisim-Evolution project, create a new schematic in the project, and implement your fully optimized circuits. Make sure to test your circuit to verify that the circuit works as you expect. Show it to your TA to actually greet them!

Note: In the Properties panel of the 7-segment display. You should choose "Yes" for "Active on High" — this means the segment is lit when the corresponding output bit is 1.

3 Lab Report

Include the following in your lab report named "`lab2report.pdf`".

- Your name, student number, and the PRA section that you're enrolled in.
- The Karnaugh-maps of the desired circuit.
- The optimized logic expressions for the circuit.
- Screenshots of your circuit diagram that demonstrate the input and output of the working circuit, i.e., there should be eight screenshots each of which shows the one of the input combination and the corresponding letter output on the 7-segment display.

4 Summary of TODOs

Below is a short summary of the steps to be completed for this lab:

1. Before the lab, generate the optimized circuit expressions using K-map.
2. In the lab, implement the circuit in Logisim-Evolution. Save it as "`lab2.circ`".
3. Test the circuit to verify that it is working correctly. Greet your TA with it.
4. Complete the lab report.
5. Submit `lab2.circ` and `lab2report.pdf` to MarkUs before the deadline.

Evaluation (2 marks in total):

- 0.5 mark for the completeness of the circuit.
- 0.5 mark for the completeness of the K-maps and the optimal logic expressions.
- 1 mark for the correct circuit behaviour.